

Model Name: Z590 UD AC

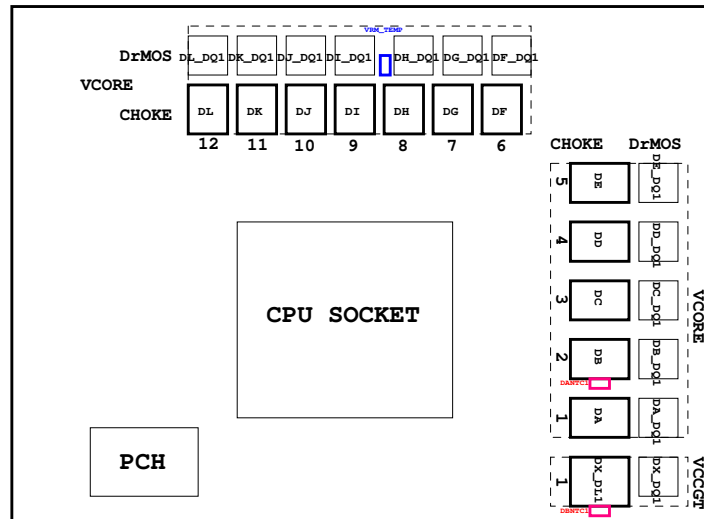
rev 1.0

SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1200-A (RKL_R0.12)
05	CPU_LGA1200-B-DDR4 (RKL_R0.12)
06	CPU_LGA1200-C (RKL_R0.12)
07	CPU_LGA1200-D (RKL_R0.12)
08	DDR 4 CHANNEL A (CML_R0.1)
09	DDR 4 CHANNEL B (CML_R0.1)
10	PCH CLK,DMI,CNVI (RKL_R0.15)
11	PCH SPI,USB (RKL_R0.15)
12	PCH PCIE,SATA (RKL_R0.15)
13	PCH ESPI,MISC (RKL_R0.15)
14	PCH GPP,HDA (RKL_R0.15)
15	PCH PWR,GND (RKL_R0.15)
16	Heatsink
17	ITE ITE8689 (RKL_R0.1)
18	HWM (RKL_R0.1)
19	FAN CTRL-CFL-SIO_5 FAN (RKL_R0.1)
20	Single BIOS for CS mode (RKL_R0.1)
21	PCI EXPRESS X16 SLOT (REV0.3)
22	PCI EXPRESS X4 SLOT (PCH) (REV0.51)
23	PCI EXPRESS X1 *3 (REV0.51)
24	SATA
25	M.2 x4 (A) (RKL_R0.1)
26	M.2 x2 (M) (RKL_R0.1)
27	M.2 x4 (P) (RKL_R0.1)
28	COM,LPT,TPM, THB (CML_R0.94)
29	ISL69269_L=0.15u (RKL_R0.1)
30	RAA229001_L=0.15u (RKL_R0.1)
31	VCORE_PSTAGE-1_L=0.15u (RKL_R0.1)
32	VCORE_PSTAGE-2_L=0.15u (RKL_R0.1)
33	VCORE_PSTAGE-3_L=0.15u (RKL_R0.1)
34	VCCGT_PSTAGE_L=0.15u (RKL_R0.1)
35	VCCSA_MOS (RKL_R0.1)
36	VCCIO-Ferrite-Z系列 (RKL_R0.2)
37	VCCIO2-Ferrite-Z系列 (RKL_R0.2)
38	RT8120_DDR_CHOKE-Ferrite-2L (RKL_R0.1)
39	RT8120_VPP_CHOKE-合金
40	NCP81269_VCC18_PCH
41	RT8068_VCC1V8_PRIM
42	DISCRETE POWER (REV0.1)
43	ATX POWER , A_-PROCHOT
44	DP PORT (RKL_R0.96)
45	CNVi_M2_WIFI (CML_R0.94)
46	Redriver_A_Type-A (RKL_R0.1)
47	R_USB30 (CML_R0.94)
48	GENESYS GL850S_1 (RKL_R0.1)
49	GENESYS GL850S_2 (RKL_R0.1)

SHEET

TITLE

50	F_USB20 (CML_R0.94)
51	F_U32 (CML_R0.94)
52	KB_MS_USB (CML_R0.94)
53	FRONT Type-C USB3.1 GEN2
54	REALTEK RTL8125BS (CML_R0.3)
55	U32_LAN CONNECTOR-8125 (CML_R0.3)
56	Realtek ALC897 (RKL_R6.0)
57	REAR AUDIO JACK (RKL_R6.0)
58	CPU POWER-1 (RKL_R0.11)
59	CPU POWER-1 (RKL_R0.11)
60	NCT3933 (RKL_R0.11)
61	F_PANEL
62	IT5702 (RKL_R1.0)
63	PCH/AUDIO/DEBUG/C_LED1/2 (RKL_R1.0)
64	D_LED1/D_LED2 (RKL_R1.0)
65	SMBUS SWITCH (RKL_R0.1)
66	CKG (RKL_R0.1)
67	EMI-ESD
68	POWER MAP
69	NTC MAP

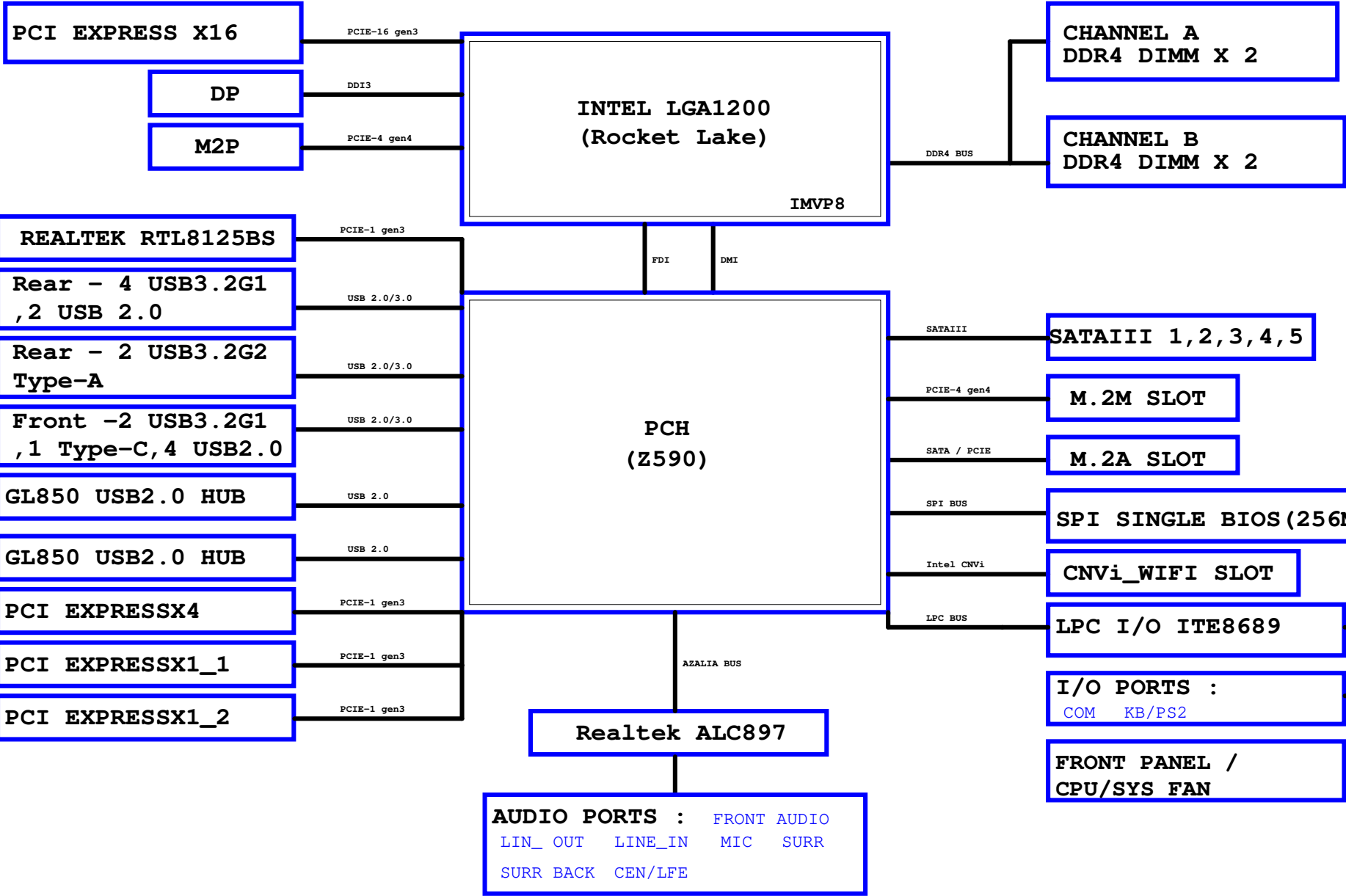


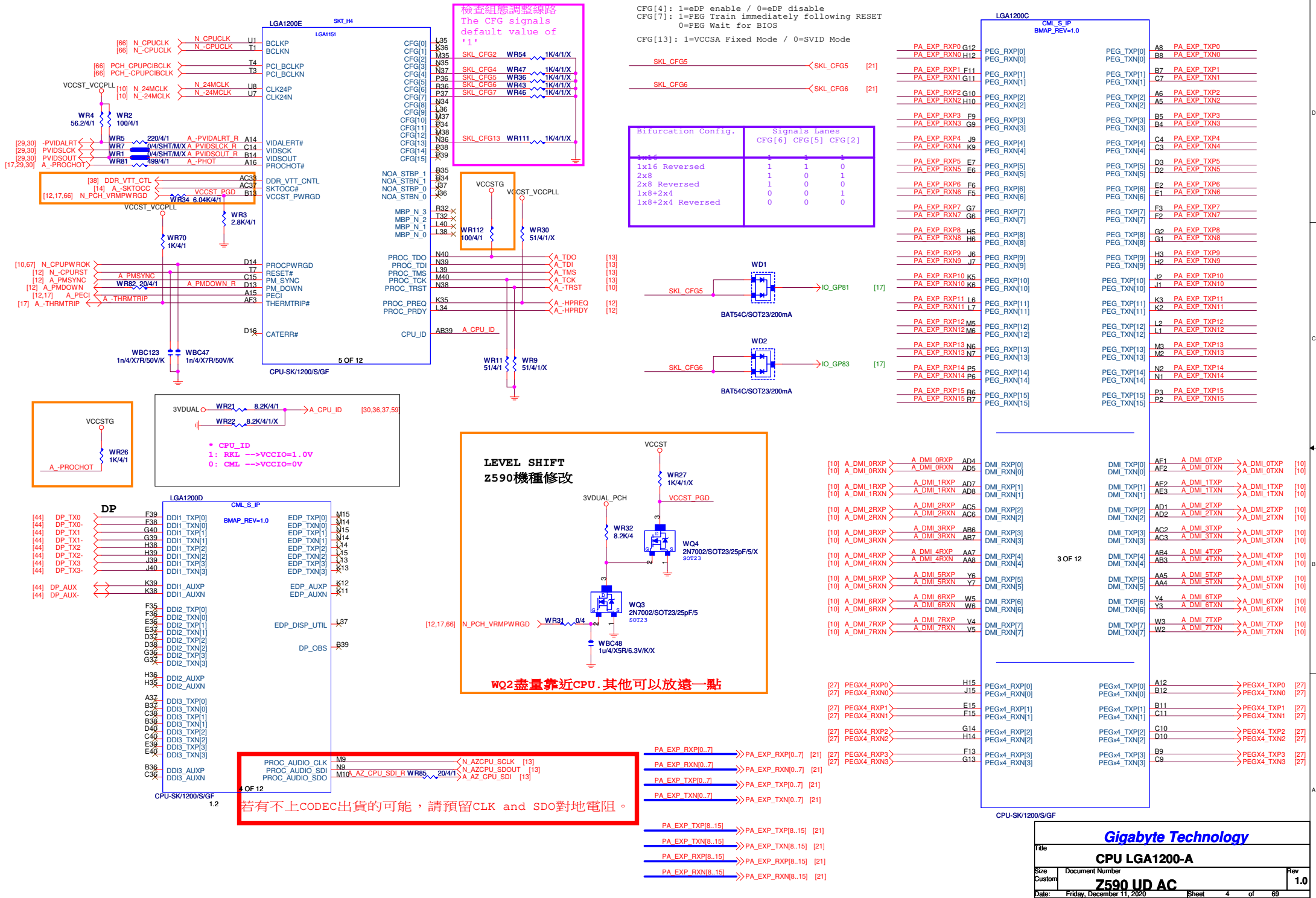
Circuit or PCB layout change

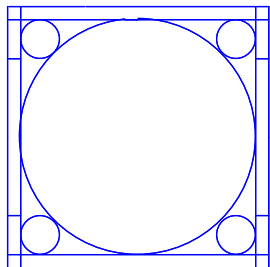
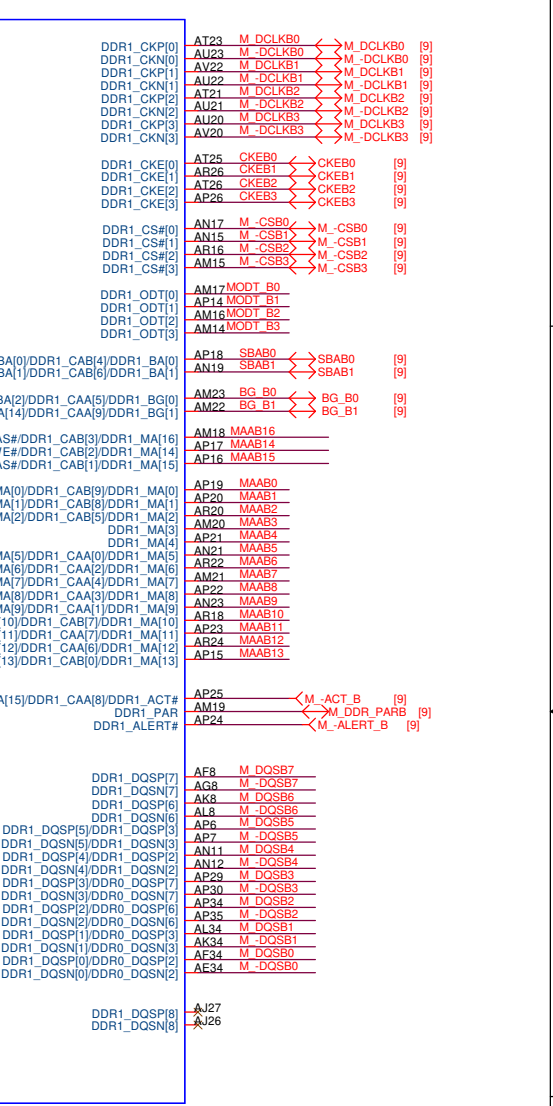
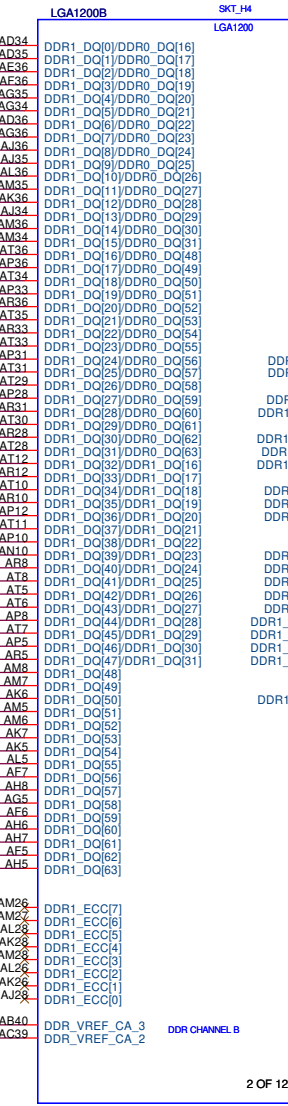
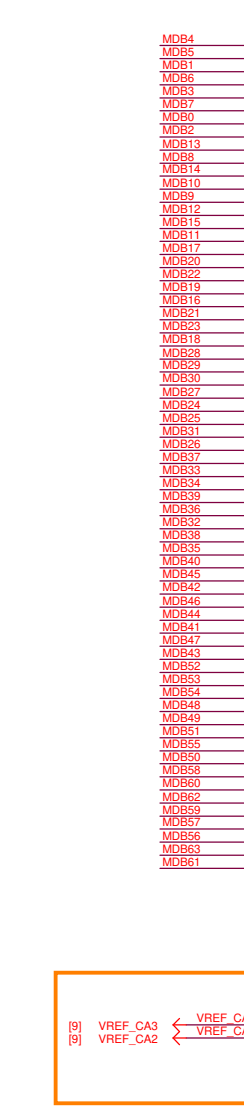
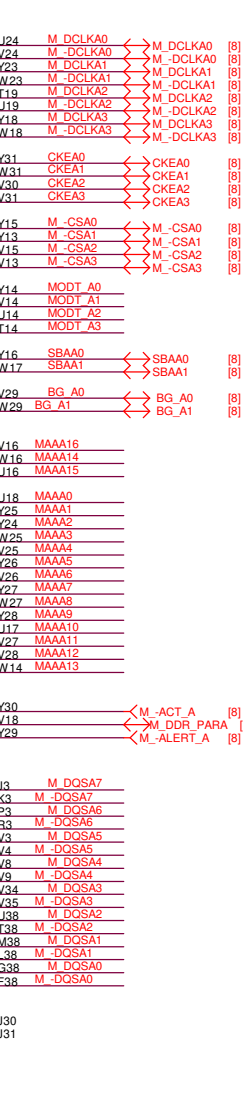
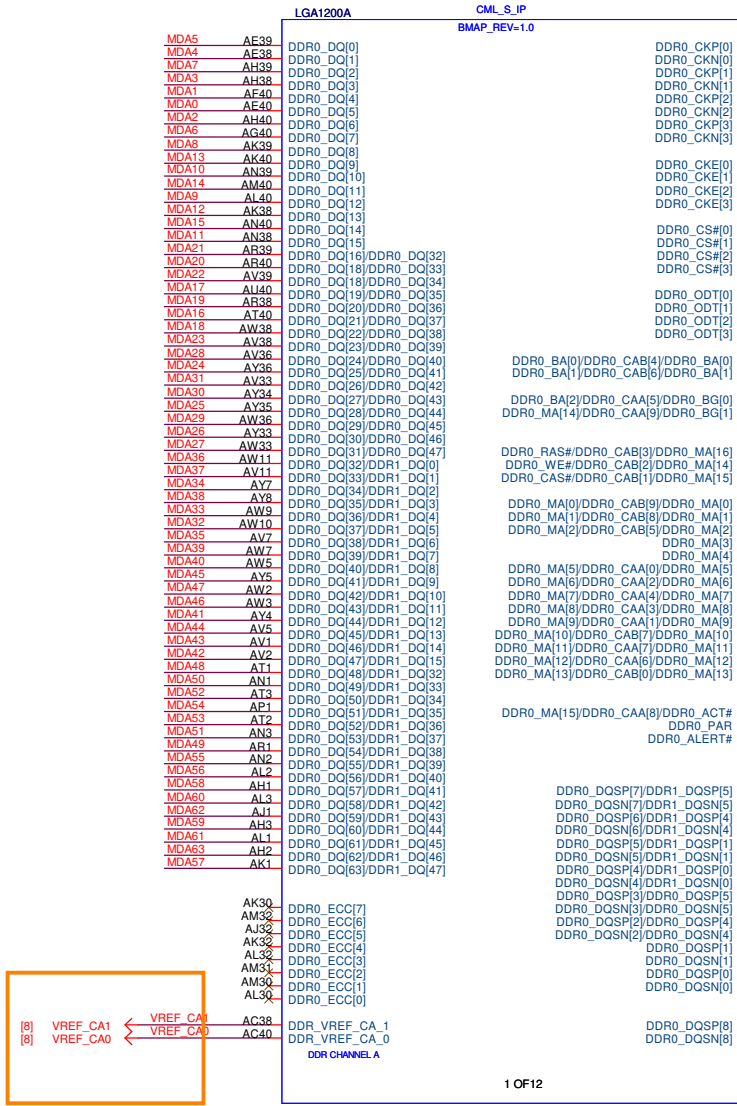
2017/07/19

[illegible]

BLOCK DIAGRAM

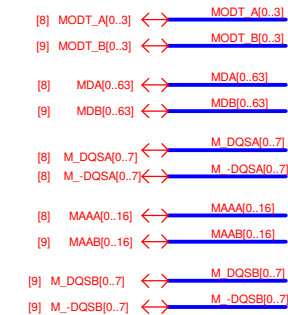






黑色cover

LGA1200
ILM_BP_CR/1200/BKN/12KRC-SF0001-83R_12KRC-SF0001-84R



Gigabyte Technology

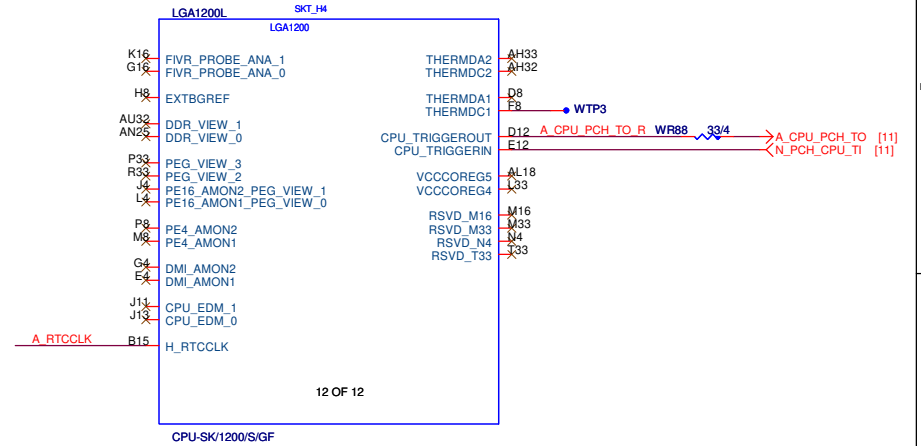
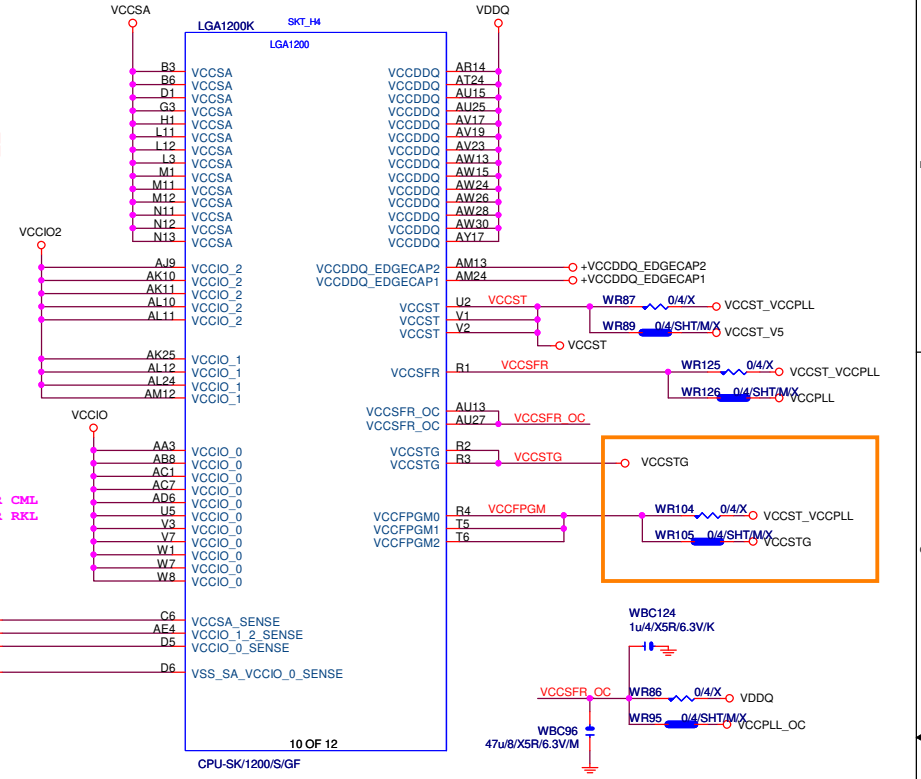
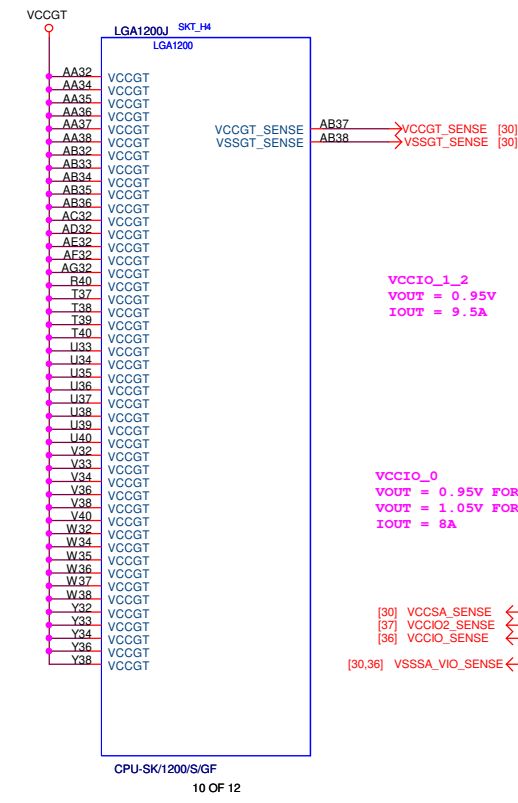
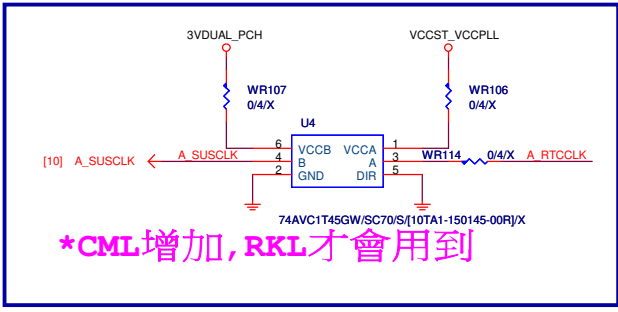
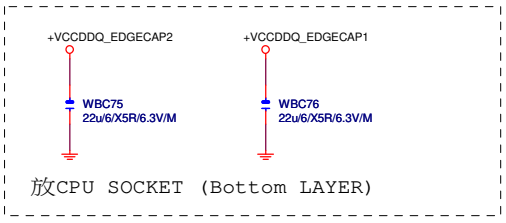
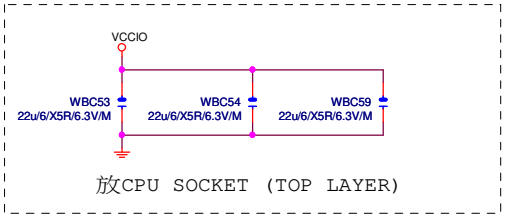
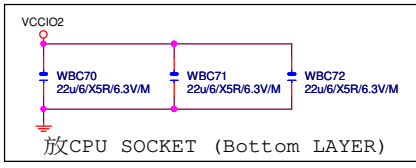
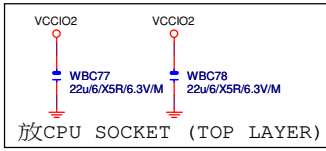
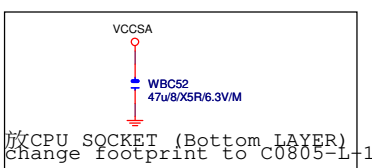
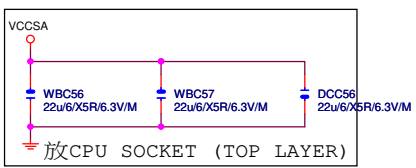
CPU LGA1200-B

Size Custom Document Number

Z590 UD AC

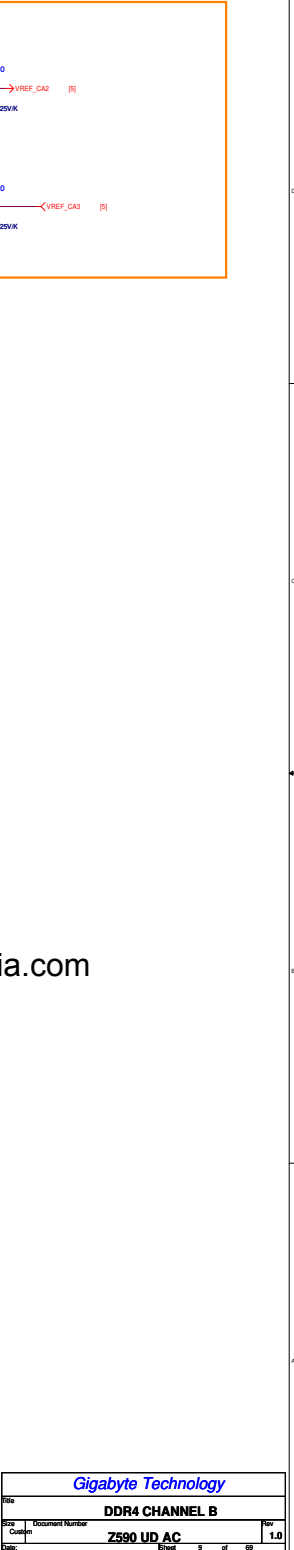
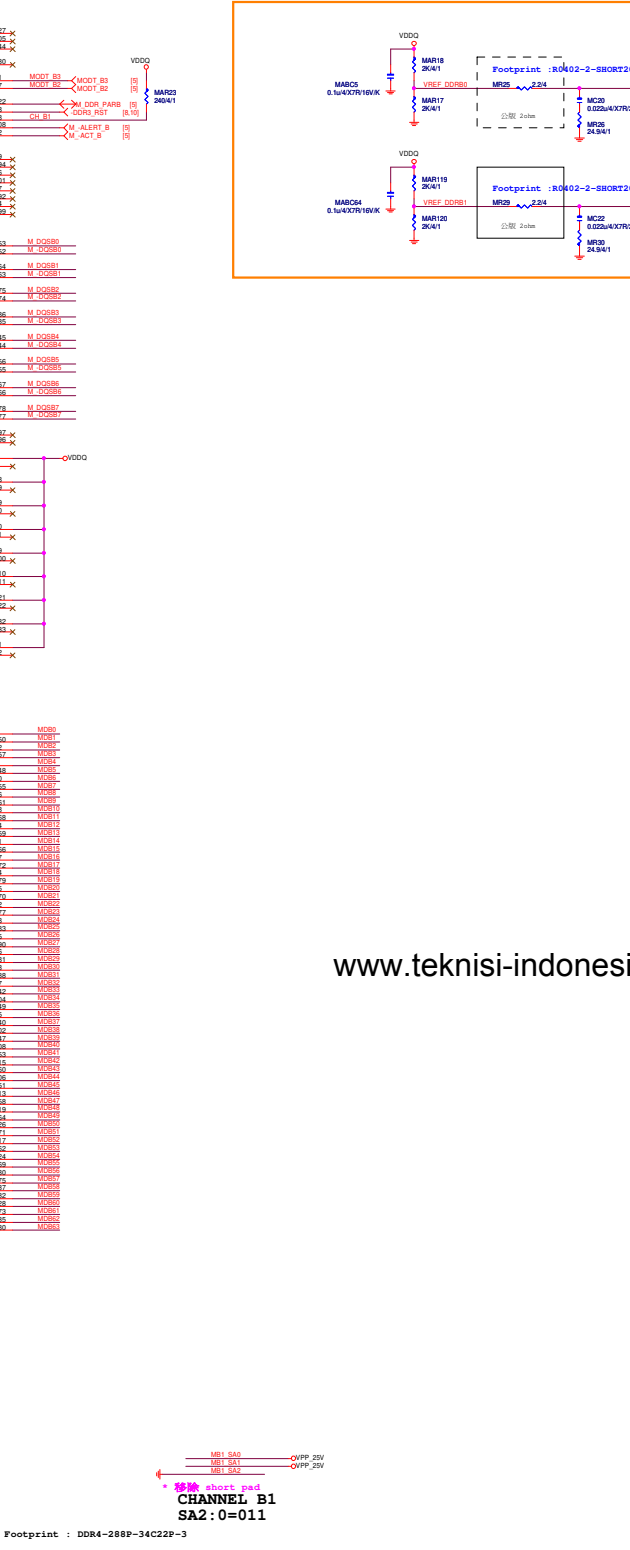
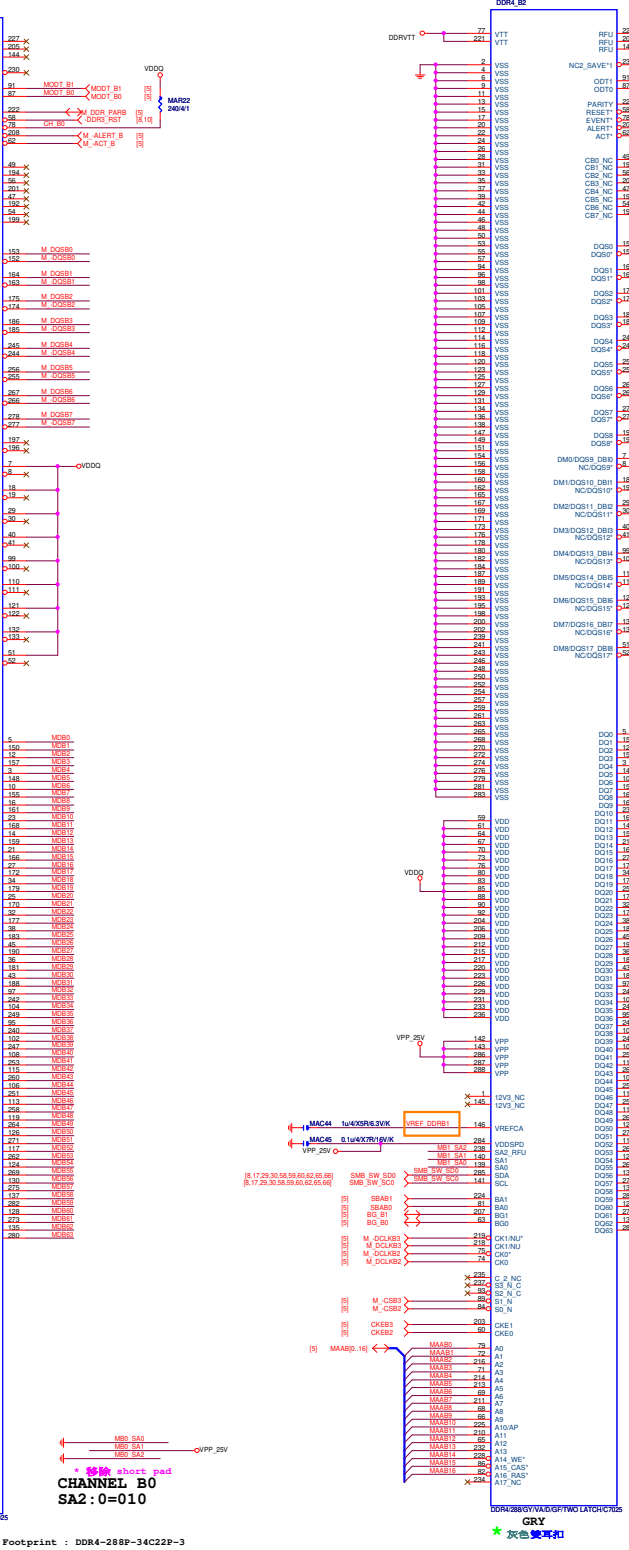
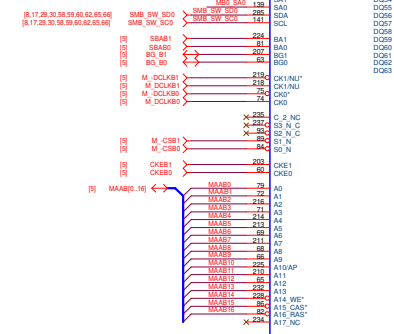
Date: Friday, December 11, 2020 Sheet 5 of 69

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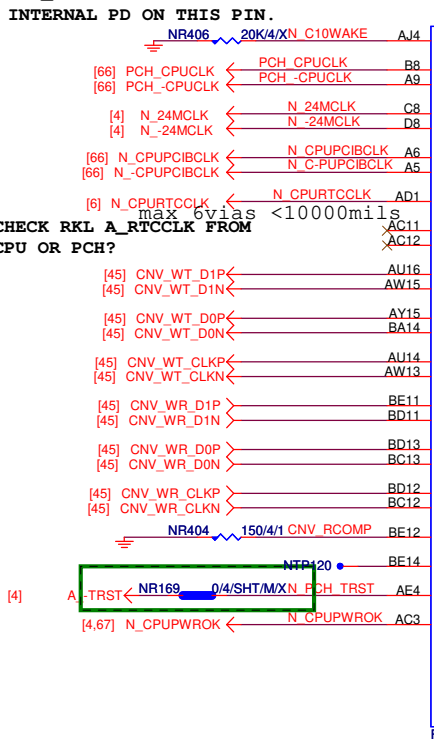




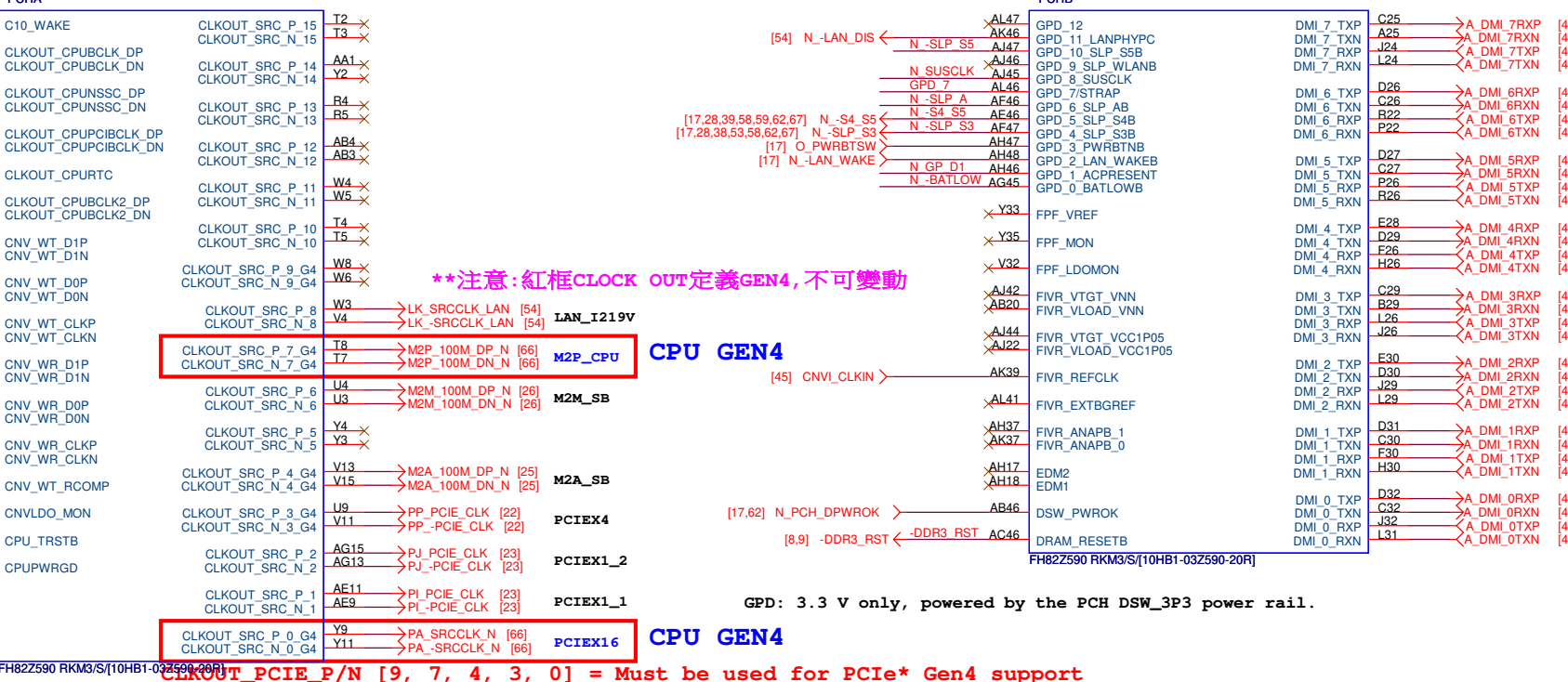
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RKL_TGP_PCH-H R0.15

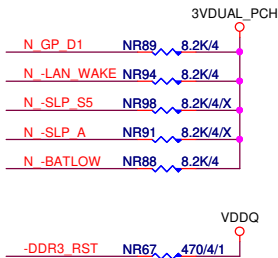
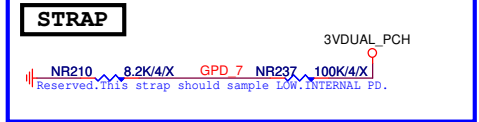
C10_WAKE RESERVED/BIOS NEED TO PROGRAM
INTERNAL PD ON THIS PIN.



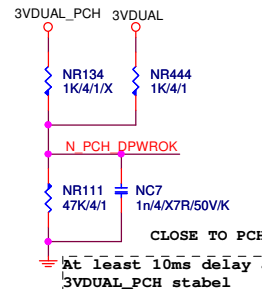
PCHB



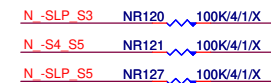
STRAP



N_SUSCLK MAX 2 LOADS SUPPORTED

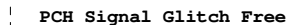


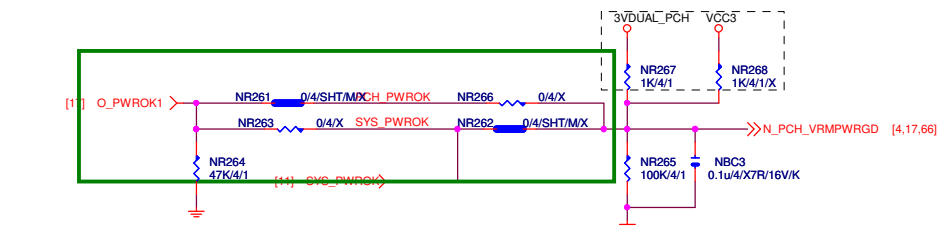
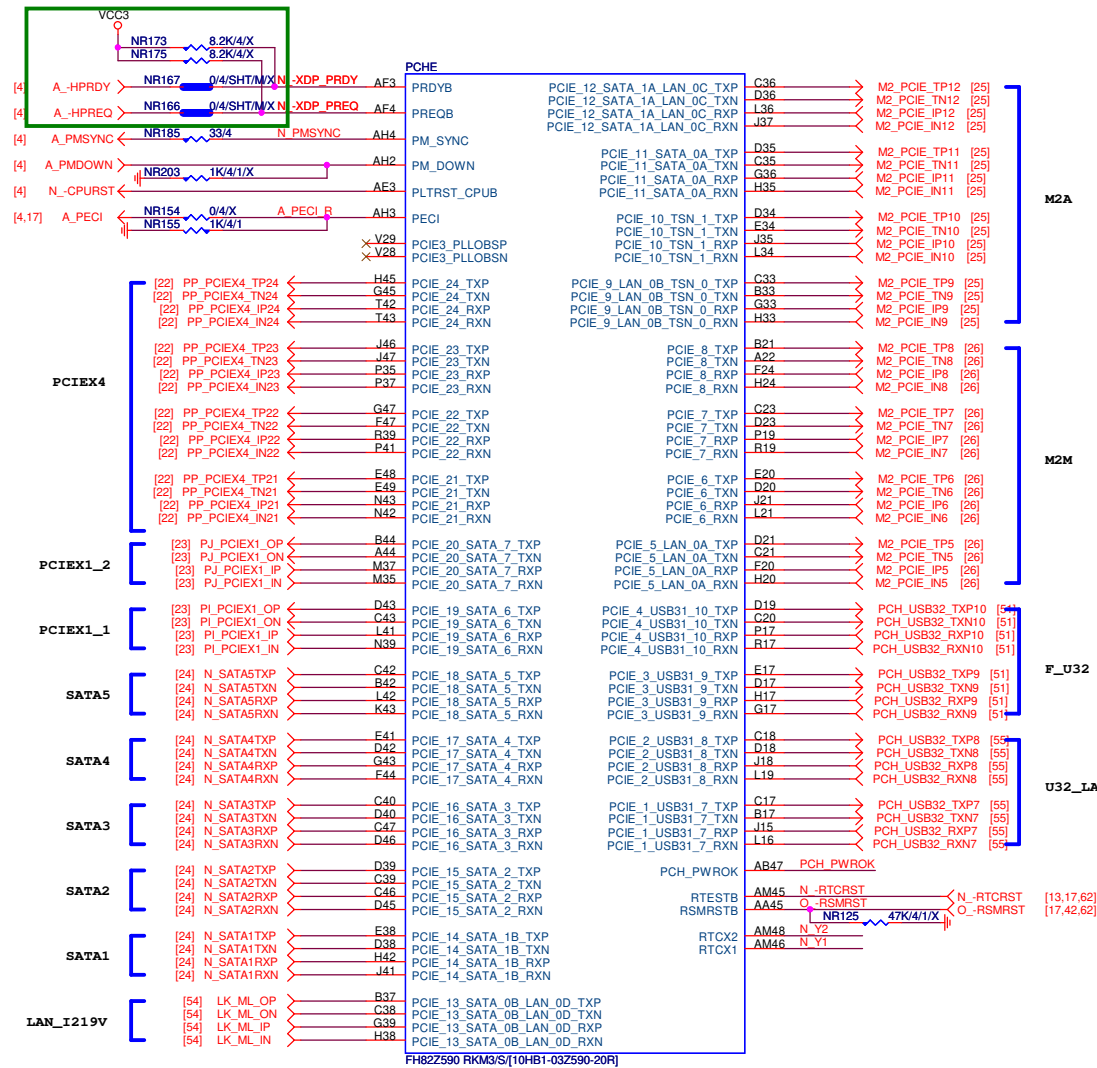
PCH Signal Glitch Free



ANS 8595665		Gigabyte Technology	
Title		PCH CLK,DMI,CNVI	
Size B	Document Number	Z590 UD AC	
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RKL_TGP_PCH-H R0.15

DC



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Intel 500 series PCH PCIE P5-P12								
ITEM	PCIE P5	PCIE P6	PCIE P7	PCIE P8	PCIE P9	PCIE P10	PCIE P11	PCIE P12
H510	PCIE /Gbe	PCIE	PCIE	PCIE	Gbe ONLY	N/A	PCIE	PCIE /Gbe
B560	PCIE /Gbe	PCIE	PCIE	PCIE	PCIE /Gbe	PCIE	PCIE SATA_0'	PCIE SATA_1' Gbe
H570	PCIE /Gbe	PCIE	PCIE	PCIE	PCIE /Gbe	PCIE	PCIE SATA_0'	PCIE SATA_1' Gbe
Z590	PCIE /Gbe	PCIE	PCIE	PCIE	PCIE /Gbe	PCIE	PCIE SATA_0'	PCIE SATA_1' Gbe
Q570	PCIE /Gbe	PCIE	PCIE	PCIE	PCIE /Gbe	PCIE	PCIE SATA_0'	PCIE SATA_1' Gbe
W580	PCIE /Gbe	PCIE	PCIE	PCIE	PCIE /Gbe	PCIE	PCIE SATA_0'	PCIE SATA_1' Gbe
					Intel® RST for x2/x4 M.2			

Intel 500 series PCH PCIE P13-P24												
ITEM	PCIE P13	PCIE P14	PCIE P15	PCIE P16	PCIE P17	PCIE P18	PCIE P19	PCIE P20	PCIE P21	PCIE P22	PCIE P23	PCIE P24
H510	SATA_0 GbE	SATA_1	SATA_2	SATA_3	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
B560	SATA_0 GbE	SATA_1	SATA_2	SATA_3	SATA_4	SATA_5	N/A	N/A	PCIE	PCIE	PCIE	PCIE
H570	PCIE SATA_0 GbE	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE	PCIE	PCIE	PCIE	PCIE	PCIE
Z590	PCIE SATA_0 GbE	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE	PCIE	PCIE	PCIE	PCIE	PCIE
Q570	PCIE SATA_0 GbE	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE	PCIE	PCIE	PCIE	PCIE	PCIE
W580	PCIE SATA_0 GbE	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE SATA_6	PCIE SATA_7	PCIE	PCIE	PCIE	PCIE
					Intel® RST for x2/x4 M.2				Intel® RST for x2/x4 M.2			

Intel 500 series PCH USB P7~P10				
ITEM	USB P7	USB P8	USB P9	USB P10
H510	NA	NA	NA	NA
B560	NA	NA	NA	NA
H570	U3.2 Gen1x1	U3.2 Gen1x1	PCIE	PCIE
Z590	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1
	PCIE	PCIE	PCIE	PCIE
Q570	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen1x1	U3.2 Gen1x1
	PCIE	PCIE	PCIE	PCIE
W580	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1
	PCIE	PCIE	PCIE	PCIE

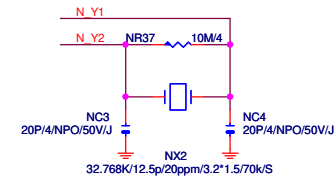
RTC 32.768KHZ

DIP X'TAL

Del DIP NX1

OPTION

SMD X'TAL

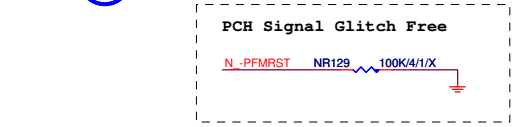


GPP_D	PU/PD
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3VDUAL

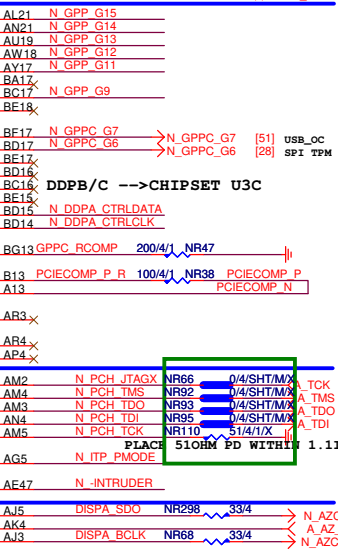
NR296 8.2K/4 N -VRALERT

N -SLP S0 NR438 100K/4/1



CLR_CMOS
N -RTCRST
PH/1*2/BK/2.54/VAD

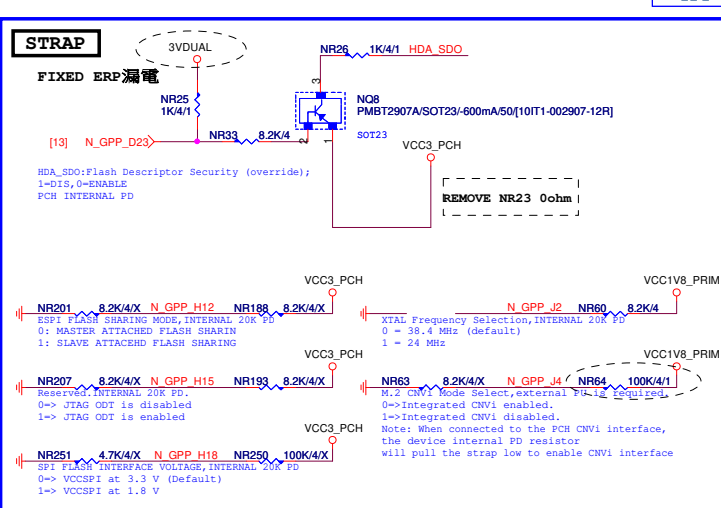
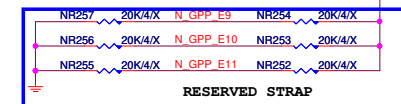
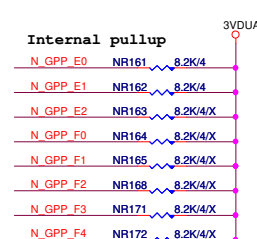
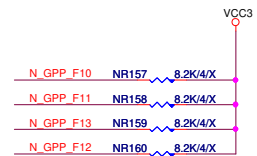
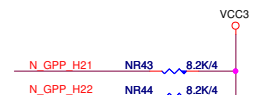
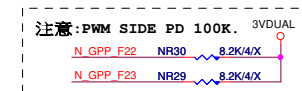
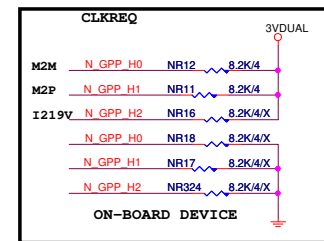
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GPP_D_21_UART3_TXD_THC1_SPI2_IO_3		GPPC_A_12_ESPI_ALERT2B
GPP_D_20_UART3_RXD_THC1_SPI2_IO_2		GPPC_A_11_ESPI_ALERT1B
GPP_D_19_GSP3_CLKI_THC1_SPI2_IO_1		GPPC_A_10_ESPI_ALERT0B
GPP_D_18_GSP3_MISO_THC1_SPI2_IO_0		GPPC_A_9_ESPI_CS3B
GPP_D_17_GSP3_CLKI_THC1_SPI2_CLK		GPPC_A_8_ESPI_CS2B
GPP_D_16_GSP3_CS0B_THC1_SPI2_CSB		GPPC_A_7_ESPI_CS1B
GPP_D_15_SML1DATA		GPPC_A_6_ESPI_RESETB
GPP_D_14_SPI1_IO_3_THC0_SPI1_IO_3		GPPC_A_5_ESPI_CLK
GPP_D_13_SPI1_IO_2_THC0_SPI1_IO_2		GPPC_A_4_ESPI_CS0B
GPP_D_12_ISH_UART0_CTSB_SML0ALERTB		GPPC_A_3_ESPI_IO_3_SUSACKB
GPP_D_11		GPPC_A_2_ESPI_IO_2_SUSWARNB_SUSWRNACKB
GPP_D_10_SML0DATA		GPPC_A_1_ESPI_IO_1
GPP_D_9_SML0CLK		GPPC_A_0_ESPI_IO_0
GPP_D_8_I2S2_SCLK_THC0_SPI1_INTB		
GPP_D_7_I2S2_RXD_THC0_SPI1_RSTB		
GPP_D_6_I2S2_TXD_MODEM_CLKREQ_CRF_XTAL_CLKREQ		STRAP/GPPC_G_15_DDP2_CTRLDATA_TBT_LSX1_B
GPP_D_5_I2S2_SFRM_CNV_RF_RESET_B		GPPC_G_14_DDP2_CTRLCLK_TBT_LSX1_A
GPP_D_4_SML1CLK		STRAP/GPPC_G_13_DDP1_CTRLDATA_TBT_LSX0_B
GPP_D_3_SPI1_MISO_IO_0_THC0_SPI1_IO_0_SBK_3_SBK4		GPPC_G_12_DDP1_CTRLCLK_TBT_LSX0_A
GPP_D_2_SPI1_MISO_IO_1_THC0_SPI1_IO_1_SBK_2_BK_2		GPPC_G_10_ISH_SPI_MISO_DDP4_CTRLCLK_GSP12_MISO_TBT_LSX3_A
GPP_D_1_SPI1_CLK_THC0_SPI1_CLK_SBK_1_BK_1		GPPC_G_9_ISH_SPI_CLK_DDP3_CTRLCLK_GSP12_CLK_TBT_LSX2_A
GPP_D_0_SPI1_CSB_THC0_SPI1_CSB_SBK_0_BK_0		GPPC_G_8_ISH_SPI_CSB_DDP3_CTRLCLK_GSP12_CS0B_TBT_LSX2_A
GPP_C_23_UART2_CTSB_CNV_MFUART0_CTS_B		GPPC_G_7
GPP_C_22_UART2_RTSB_CNV_MFUART0_RTS_B		GPPC_G_6
GPP_C_21_UART2_TXD_CNV_MFUART0_TXD		GPPC_G_5_SLP_DRAMB
GPP_C_20_UART2_RXD_CNV_MFUART0_RXD		GPPC_G_4_GMII_MDIO_0
GPP_C_19_I2C1_SCL		GPPC_G_3_GMII_MDC_0
GPP_C_18_I2C1_SDA		GPPC_G_2_DNX_FORCE_RELOAD
GPP_C_17_I2C0_SCL		GPPC_G_1_GDPA_CTRLDATA
GPP_C_16_I2C0_SDA		GPPC_G_0_DDP4_CTRLCLK
GPP_C_15_UART1_CTSB_ISH_UART1_CTSB		
GPP_C_14_UART1_RTSB_ISH_UART1_RTSB		GPPC_RCOMP
GPP_C_13_UART1_TXD_ISH_UART1_TXD		MPHY_RCOMPMP
GPP_C_12_UART1_RXD_ISH_UART1_RXD		MPHY_RCOMPNP
GPP_C_11_UART0_CTSB		
GPP_C_10_UART0_RTSB		MLK_RSTB
GPP_C_9_UART0_TXD		
GPP_C_8_UART0_RXD		
GPP_C_7_ISH_I2C2_SCL_I2C3_SCL		MLK_DATA
GPP_C_6_ISH_I2C2_SDA_I2C3_SDA_SBK_4_BK_4		MLK_CLK
GPP_C_5_SML0ALERTB/STRAP		
GPP_C_4_ISH_UART0_TXD_SML0BCLK_I2C2_SCL		JTAGX
GPP_C_3_ISH_UART0_RXD_SML0BDATA_I2C2_SDA		JTAG_TMS
GPP_C_2_SMBALERTB/STRAP		JTAG_TDO
GPP_C_1_SMBDATA		JTAG_TDI
GPP_C_0_SMBCLK		JTAG_TCK
GPP_B_23_SML1ALERTB_PCHHOTB/STRAP		STRAP/DBG_PMODE
GPP_B_22_GSP11_MOSI/STRAP		
GPP_B_21_GSP11_MISO_NFC_CLKREQ		INTRUDERB
GPP_B_20_GSP11_CLK_NFC_CLK		
GPP_B_19_GSP11_CS0B		HDACPU_SDO
GPP_B_18_GSP11_MOSI/STRAP		HDACPU_SDI
GPP_B_17_GSP10_MISO		IN_HDACPU_BCLK
GPP_B_16_GSP10_CLK		
GPP_B_15_GSP10_CS0B		
GPP_B_14_SPKR/STRAP		
GPP_B_13_PLTRSTB		
GPP_B_12_SLP_S0B		
GPP_B_11_I2S_MCLK		
GPP_B_10_SRCCCLKREQB_5		
GPP_B_9_SRCCCLKREQB_4		
GPP_B_8_SRCCCLKREQB_3		
GPP_B_7_SRCCCLKREQB_2		
GPP_B_6_SRCCCLKREQB_1		
GPP_B_5_SRCCCLKREQB_0		
GPP_B_4_CPU_GP_3		
GPP_B_3_CPU_GP_2		
GPP_B_2_VREALERTB		
GPP_B_1_GSP11_CS1B_TIME_SYNC_1		
GPP_B_0_GSP10_CS1B		

[illegible]

The schematic diagram illustrates the VCC3 power plane. It features a central horizontal rail labeled VCC3. To the left, a red box highlights the connection to VCC3_PCH, which is terminated with an 8.2K/4X resistor. Below this, a V1P05A component is shown. To the right, the 3VDUAL input is connected to the VCC3 rail. Various components are connected to the VCC3 rail, including N_GPP_G12 NR275 (terminated with a 3.3K/4/1 resistor), N_SMBCLK NR53 (1K/4/1), N_SMBDATA NR55 (1K/4/1), N_SML0CLK NR58 (499/4/1), N_SML0DAT NR59 (499/4/1), N_SML1DAT NR61 (8.2K/4), N_SML1CLK NR29 (8.2K/4), N_GPP_D3 NR52 (8.2K/4), and N_GPCC_G7 NR71 (8.2K/4).

ANS 8595665		<i>Gigabyte Technology</i>	
Title			
PCH ESPI,MISC			
Size	Document Number		Rev
Custom	Z590 UD AC		1.0
Date:	Monday, January 25, 2021	Sheet	13 of 69

RKL_TGP_PCH-H R0.15



Fixed voltage on certain GPIO groups: GPD (3.3 V), GPP_J and GPP_S (1.8 V/VCCPRIM_1P8)

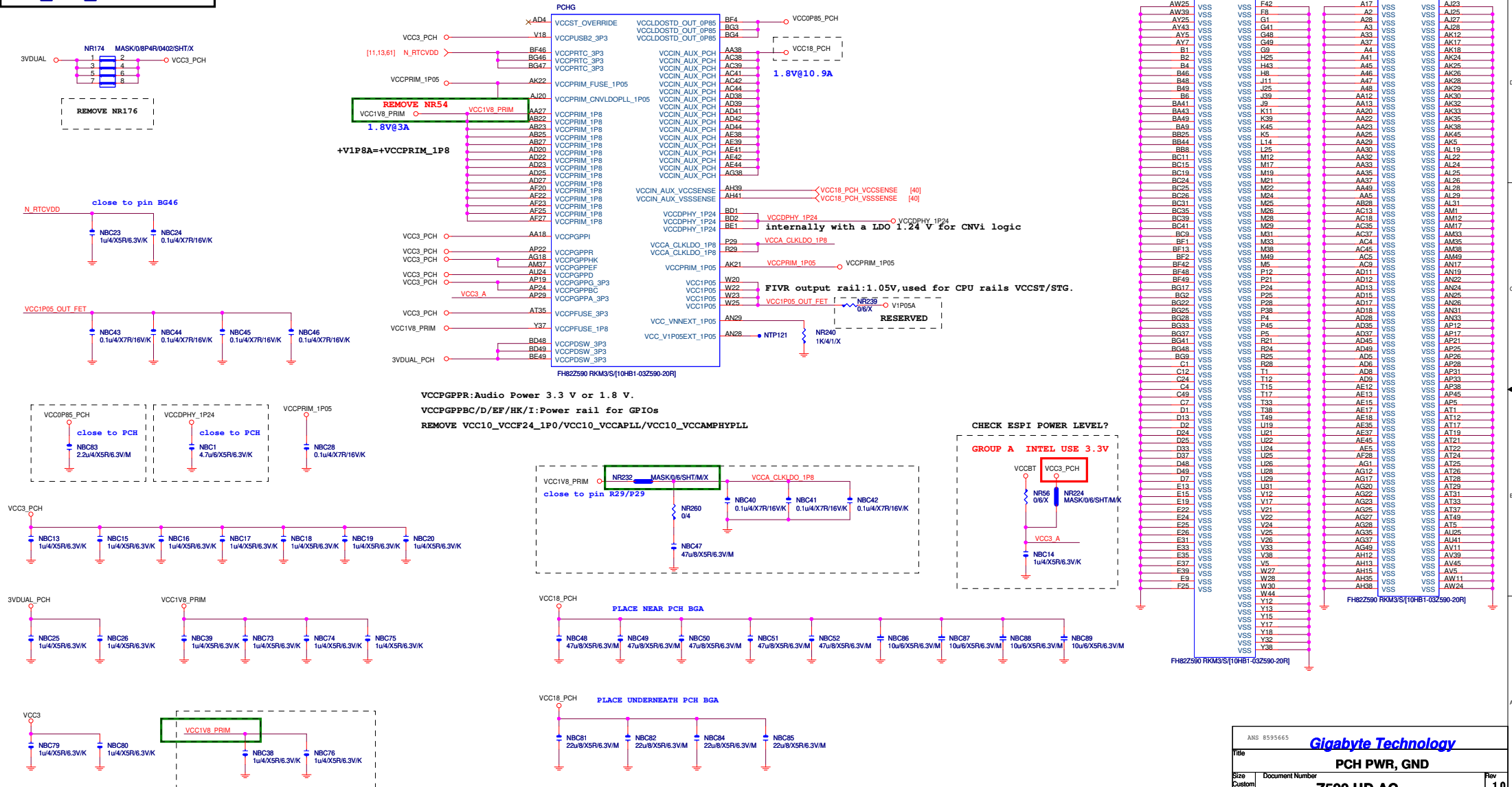
Display Port DDC/HOT PLUG SIGNAL		
CPU PORT	PCH DDC	PCH HPD
DDI_A/EDP	GPP_G0/G1	GPP_K6
DDI_1/B	GPP_I5/I6	GPP_K7
DDI_2/C	GPP_G12/G13	GPP_I1
DDI_3/D	GPP_G14/G15	GPP_I2

PCH Signal Glitch Free

CPU_VCCIO_PWR_GATEB NR28 75K/4/1/

HPD: DDI*. PULL DOWN IF NO USE.

N_GPP_K6	NR233	100K/4/1
N_GPP_K7	NR236	100K/4/1/X
N_GPP_K10	NR273	100K/4/1
N_GPP_I1	NR238	100K/4/1
N_GPP_I2	NR270	100K/4/1
N_GPP_I3	NR272	100K/4/1
N_GPP_I4	NR271	100K/4/1



裝甲HEATSINK 分成四大部份

MOS_HS

Location: TMOS 12SP2-S09840-01R/02R/03R/04R
Location: RMOS 12SP2-S09423-11R/12R/13R/14R

TMOS
TMOS_Heatsink[12SP2-S09840-01R_12SP2-S09840-02R_12SP2-S09840-03R_12SP2-S09840-04R]

RMOS
RMOS_HS[12SP2-S09423-11R_12SP2-S09423-12R_12SP2-S09423-13R_12SP2-S09423-14R]

Footprint :
SINK_Z490_UD-R

Footprint :
SINK_Z590_UD_AC-T

PCH_HS

Location: PCH_HS 12SP2-S08604-21R/22R/23R/24R

PCH_HS

Footprint :
BGHSINK-Z370_HD3P

後窗鐵片

Location: IO_SH
UD 11AIO-010061-12R
UD AC 11AIO-010061-02R

IO_SH

IO

IO[11AIO-010061-02R]

*UD與UD AC鐵片不同

裝甲

Location: REAR_HS 12KRC-0H0047-11R

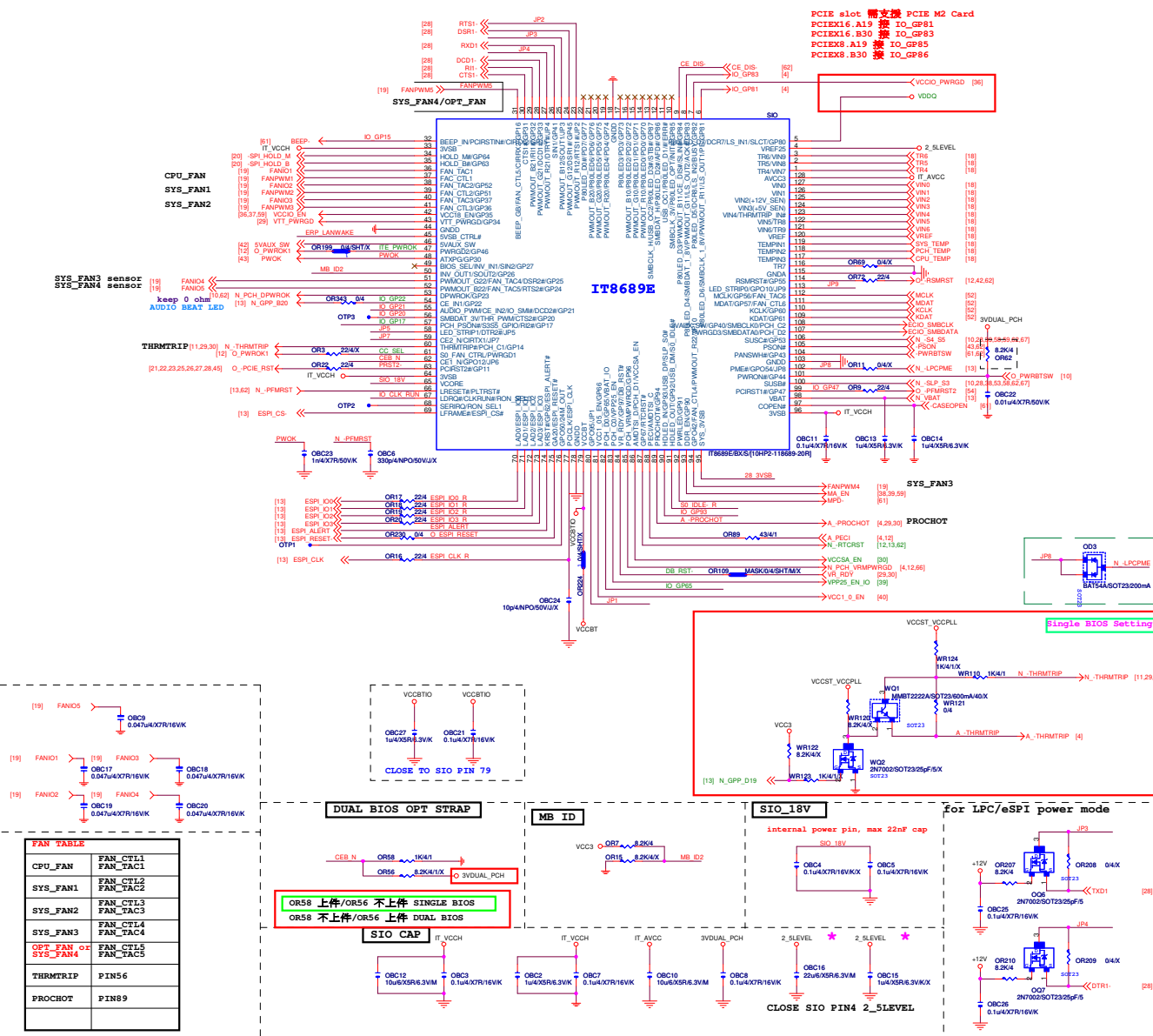
REAR_HS

Footprint :
Z490_UD_IO_COVER

- * PCB顏色 : 咖啡黑
- * 文字面 : 灰色
- * 疊構 : 2E7 (2OZ)
- * 圖騰: ID設計Z590版GIGABYTE UD

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Gigabyte Technology			
Title Heatsink			
Size Custom	Document Number Z590 UD AC		Rev 1.0
Date:	Wednesday, December 09, 2020	Sheet 1	16 of 69



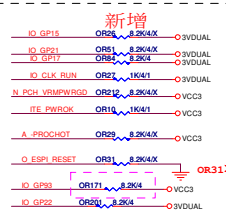
PWR SHT



請依開案規格，選擇Support Exp下 LAN Wake up組態。

(組態一) PCIE LAN (Single & Dual LAN)

SIO PU

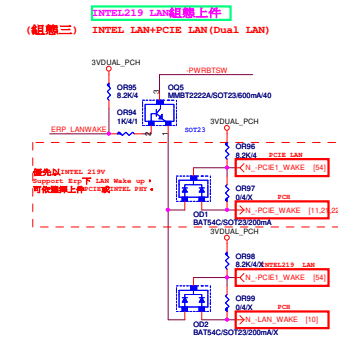


(組態二) INTEL219 LAN (Single LAN)

SIO STRAP

for eSPI

JP2	1	Disable WDT to rest PWROK
JP3 <td>0<td>Enable WDT to rest PWROK</td></td>	0 <td>Enable WDT to rest PWROK</td>	Enable WDT to rest PWROK
JP4 <td>1</td> <td>Dual-BIOS CS pin mode select bit '0'</td>	1	Dual-BIOS CS pin mode select bit '0'
JP5 <td>0</td> <td>LPCESPI power VCCBT = 3.3V</td>	0	LPCESPI power VCCBT = 3.3V
JP6 <td>1</td> <td>LPCESPI power VCCBT = 1.8V</td>	1	LPCESPI power VCCBT = 1.8V
JP7 <td>0</td> <td>LPC I/F</td>	0	LPC I/F
JP8 <td>1</td> <td>ESPI I/F</td>	1	ESPI I/F
JP9 <td>1</td> <td>Enable Dual BIOS Function (for GigaByte Only)</td>	1	Enable Dual BIOS Function (for GigaByte Only)
JP10 <td>0</td> <td>Disable Dual BIOS Function (for GigaByte Only)</td>	0	Disable Dual BIOS Function (for GigaByte Only)
JP11 <td>1</td> <td>Dual-BIOS CE pin mode select bit '1'</td>	1	Dual-BIOS CE pin mode select bit '1'
JP12 <td>0</td> <td>See the below table</td>	0	See the below table
JP13 <td>1</td> <td>CE pin disable (Hold pin mode)</td>	1	CE pin disable (Hold pin mode)
JP14 <td>0</td> <td>CE mode 1</td>	0	CE mode 1
JP15 <td>1</td> <td>CE mode 2</td>	1	CE mode 2
JP16 <td>0</td> <td>CE mode 3</td>	0	CE mode 3



ERP Wake on LAN		
Single LAN	Realtek	組態一
	Atheros	組態二
Dual LAN (只留一欄 LAN交換ERP下 WAKE UP)	Intel 219	組態一
	Atheros+Realtek	組態二
No Support ERP	Intel 219+Intel 210	組態三
	Single LAN BOM上OR97 + Dual LAN BOM上OR97 + OR99 +	

[17] VREF

[17] TR4

[17] TR5

[17] TR6

OC17 1u4/X5R/6.3V/K

X16_TEMP1 10K/1/4/S

OC14 1u4/X5R/6.3V/K

VRM_TEMP 100K/1/4/S

OC15 1u4/X5R/6.3V/K

SYS_TEMP2 10K/1/4/S

CLOSE VCORE MOSFET

OR211 10K/4/1

OR83 10K/4/1

OR85 10K/4/1

[illegible][illegible]

VCC_SIO V

OR82

0/4/SHT/X

Rev:0.6

FOR EMI ONLY

+12V

C3
1n4/X7R/50V/M

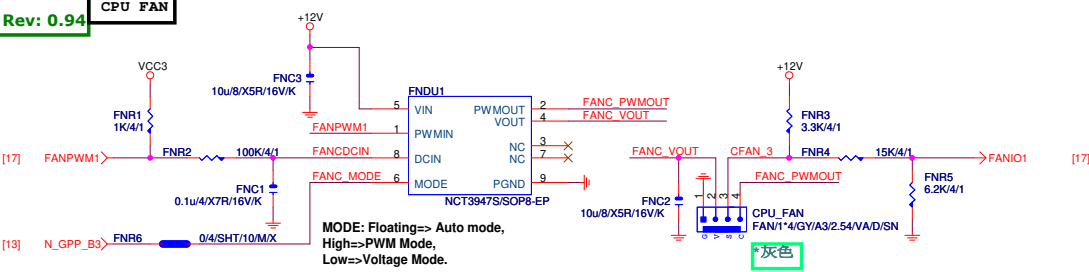
FOR EMI ONLY

VCC3

C2
0.1u/4/X7R/16V

★Update 2015-04.24

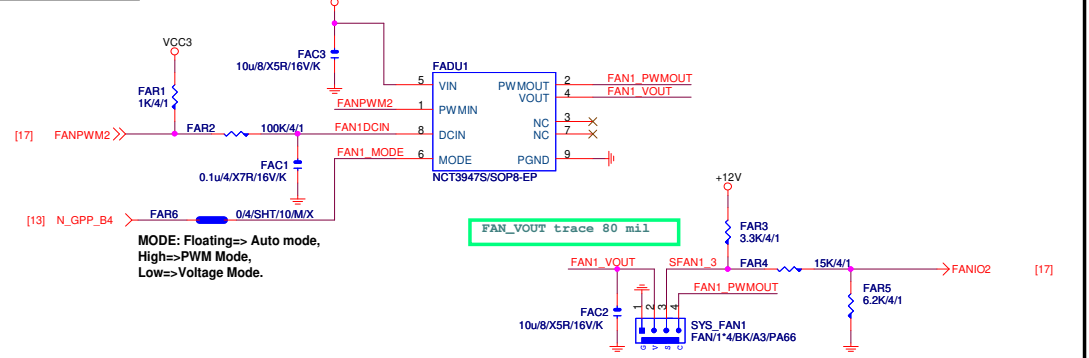
CPU_FAN



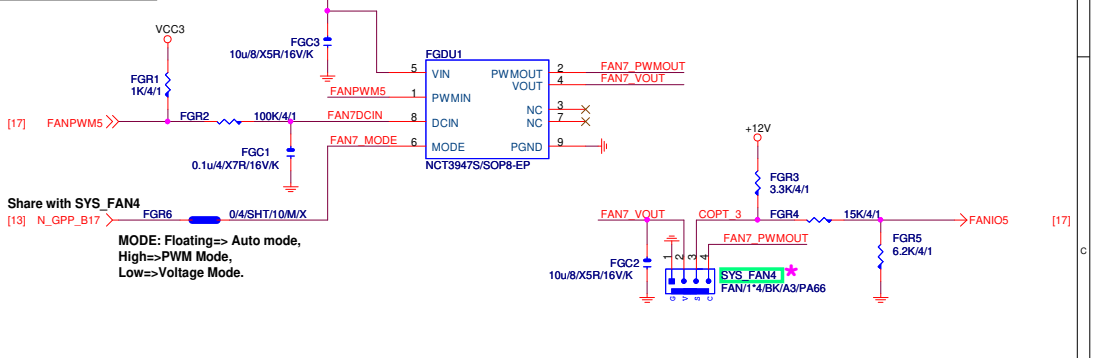
IO 4_FAN

CPU_FAN
SYS_FAN1
SYS_FAN2
SYS_FAN3
SYS_FAN4

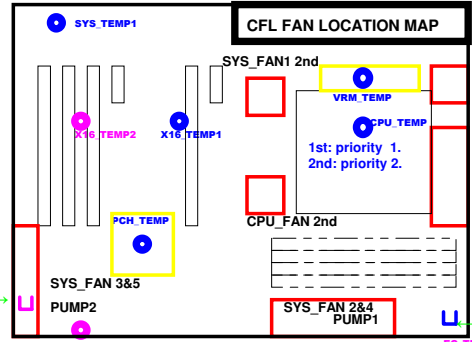
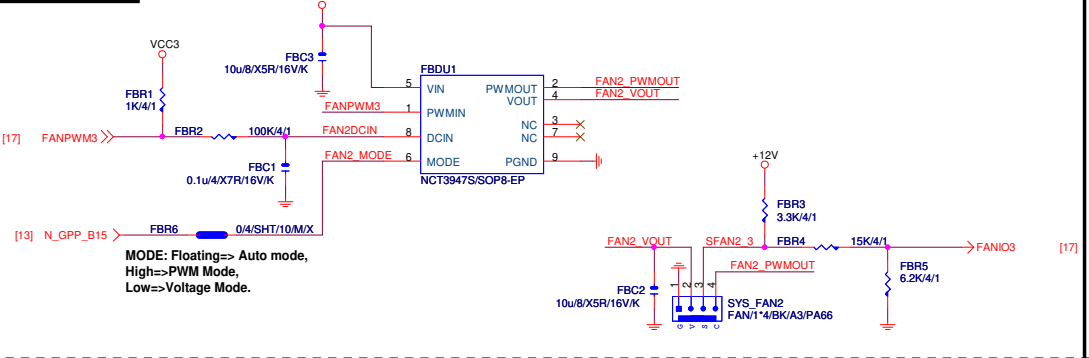
SYSTEM FAN1



SYSTEM FAN4



SYSTEM FAN2



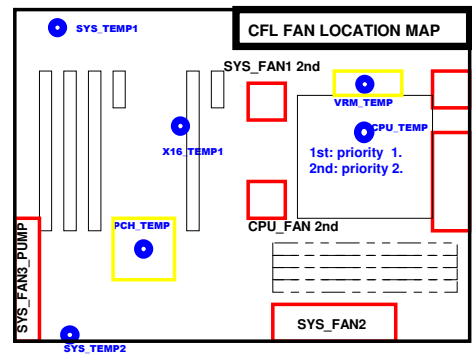
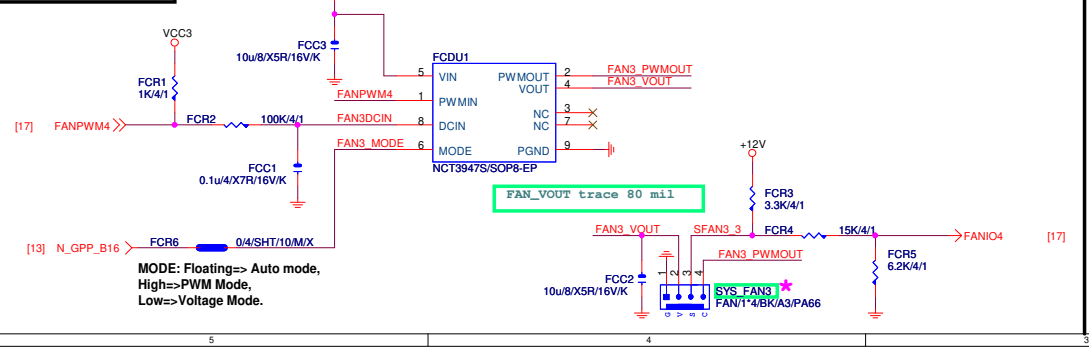
8 FAN from IO & EC

EC TEMP SENSE 879X

IO TEMP SENSE 8686

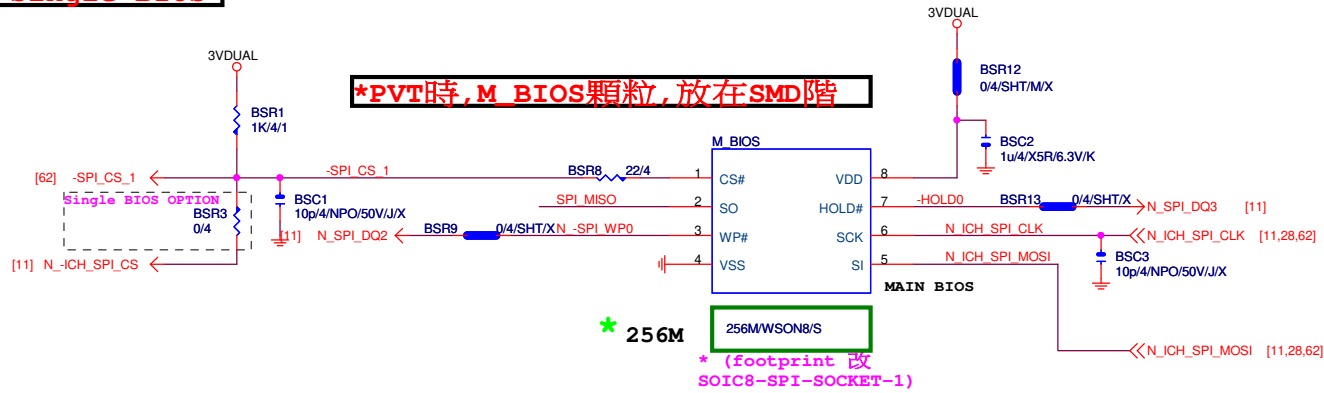
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SYSTEM FAN3

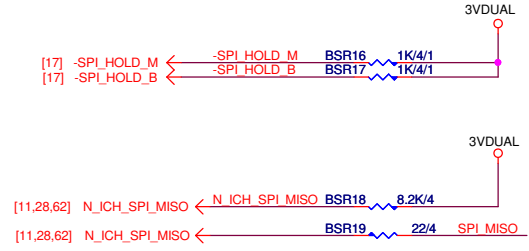


DUAL BIOS

***Single BIOS**

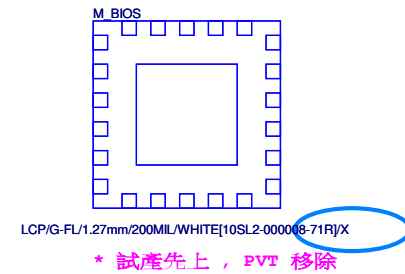


MOSI For DMI RX Termination Voltage



BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

1 means floating
0 means PD 1K



Rev 0.3

PCIEX16 CAP

PCIEX16 SLOT

PCIESLOT-1645TH

FOR SMBUS

PCIEX16不能short pad

[22,23,65] SMB_SW_SC1

[22,23,65] SMB_SW_SD

[11,17,22,23] N_PCIE_WAKE

-PCIEX16_PR

PA_EXP_TXP0_C

PA_EXP_TXN0_C

[13] -PCIEX16_PR

PA_EXP_TXP1_C

PA_EXP_TXN1_C

PA_EXP_TXP2_C

PA_EXP_TXN2_C

PA_EXP_TXP3_C

PA_EXP_TXN3_C

PA_EXP_TXP4_C

PA_EXP_TXN4_C

PA_EXP_TXP5_C

PA_EXP_TXN5_C

PA_EXP_TXP6_C

PA_EXP_TXN6_C

PA_EXP_TXP8_C

PA_EXP_TXN8_C

PA_EXP_TXP9_C

PA_EXP_TXN9_C

PA_EXP_TXP10_C

PA_EXP_TXN10_C

PA_EXP_TXP11_C

PA_EXP_TXN11_C

PA_EXP_TXP12_C

PA_EXP_TXN12_C

PA_EXP_TXP13_C

PA_EXP_TXN13_C

PA_EXP_TXP14_C

PA_EXP_TXN14_C

PA_EXP_TXP15_C

PA_EXP_TXN15_C

-PCIEX16_PR

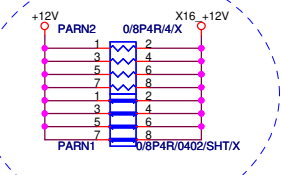
3GIO_*16

KEY

PCI-E16X-164P/BK/LONG DOUBLE/HK*2/SHELL/GEN4.0

黑色金屬加強

PCIEX16 PROTECT SHT

+12 protect
short-wire test

PCIEX16 AC CAP

PA_EXP_TXP0	PAC5	0.22u4/X5R/6.3V/K	PA_EXP_TXP0_C
PA_EXP_TXN0	PAC4	0.22u4/X5R/6.3V/K	PA_EXP_TXN0_C
PA_EXP_TXP1	PAC6	0.22u4/X5R/6.3V/K	PA_EXP_TXP1_C
PA_EXP_TXN1	PAC7	0.22u4/X5R/6.3V/K	PA_EXP_TXN1_C
PA_EXP_TXP2	PAC8	0.22u4/X5R/6.3V/K	PA_EXP_TXP2_C
PA_EXP_TXN2	PAC9	0.22u4/X5R/6.3V/K	PA_EXP_TXN2_C
PA_EXP_TXP3	PAC10	0.22u4/X5R/6.3V/K	PA_EXP_TXP3_C
PA_EXP_TXN3	PAC11	0.22u4/X5R/6.3V/K	PA_EXP_TXN3_C
PA_EXP_TXP4	PAC12	0.22u4/X5R/6.3V/K	PA_EXP_TXP4_C
PA_EXP_TXN4	PAC13	0.22u4/X5R/6.3V/K	PA_EXP_TXN4_C
PA_EXP_TXP5	PAC14	0.22u4/X5R/6.3V/K	PA_EXP_TXP5_C
PA_EXP_TXN5	PAC15	0.22u4/X5R/6.3V/K	PA_EXP_TXN5_C
PA_EXP_TXP6	PAC16	0.22u4/X5R/6.3V/K	PA_EXP_TXP6_C
PA_EXP_TXN6	PAC17	0.22u4/X5R/6.3V/K	PA_EXP_TXN6_C
PA_EXP_TXP7	PAC18	0.22u4/X5R/6.3V/K	PA_EXP_TXP7_C
PA_EXP_TXN7	PAC19	0.22u4/X5R/6.3V/K	PA_EXP_TXN7_C
PA_EXP_TXP8	PAC20	0.22u4/X5R/6.3V/K	PA_EXP_TXP8_C
PA_EXP_TXN8	PAC21	0.22u4/X5R/6.3V/K	PA_EXP_TXN8_C
PA_EXP_TXP9	PAC22	0.22u4/X5R/6.3V/K	PA_EXP_TXP9_C
PA_EXP_TXN9	PAC23	0.22u4/X5R/6.3V/K	PA_EXP_TXN9_C
PA_EXP_TXP10	PAC24	0.22u4/X5R/6.3V/K	PA_EXP_TXP10_C
PA_EXP_TXN10	PAC25	0.22u4/X5R/6.3V/K	PA_EXP_TXN10_C
PA_EXP_TXP11	PAC26	0.22u4/X5R/6.3V/K	PA_EXP_TXP11_C
PA_EXP_TXN11	PAC27	0.22u4/X5R/6.3V/K	PA_EXP_TXN11_C
PA_EXP_TXP12	PAC28	0.22u4/X5R/6.3V/K	PA_EXP_TXP12_C
PA_EXP_TXN12	PAC29	0.22u4/X5R/6.3V/K	PA_EXP_TXN12_C
PA_EXP_TXP13	PAC30	0.22u4/X5R/6.3V/K	PA_EXP_TXP13_C
PA_EXP_TXN13	PAC31	0.22u4/X5R/6.3V/K	PA_EXP_TXN13_C
PA_EXP_TXP14	PAC32	0.22u4/X5R/6.3V/K	PA_EXP_TXP14_C
PA_EXP_TXN14	PAC33	0.22u4/X5R/6.3V/K	PA_EXP_TXN14_C
PA_EXP_TXP15	PAC34	0.22u4/X5R/6.3V/K	PA_EXP_TXP15_C
PA_EXP_TXN15	PAC35	0.22u4/X5R/6.3V/K	PA_EXP_TXN15_C

PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWIDTH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWIDTH=2.5GHz*(8b/10b) X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWIDTH=2.5GHz*(8b/10b) X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWIDTH=2.5GHz*(8b/10b) X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

PCE-E X1(單向) BANDWIDTH=5GHz*(8b/10b)=4Gb/s=500MB/s

PCI-E REV:3.0--> 8GHZ

PCE-E X1(單向) BANDWIDTH=8GHz*(128b/130b)=8Gb/s=1GB/s

Gigabyte Technology		
PCI EXPRESS * 16		
Title	Document Number	Rev
	Z590 UD AC	1.0
Date:	Friday, December 11, 2020	Sheet 21 of 69

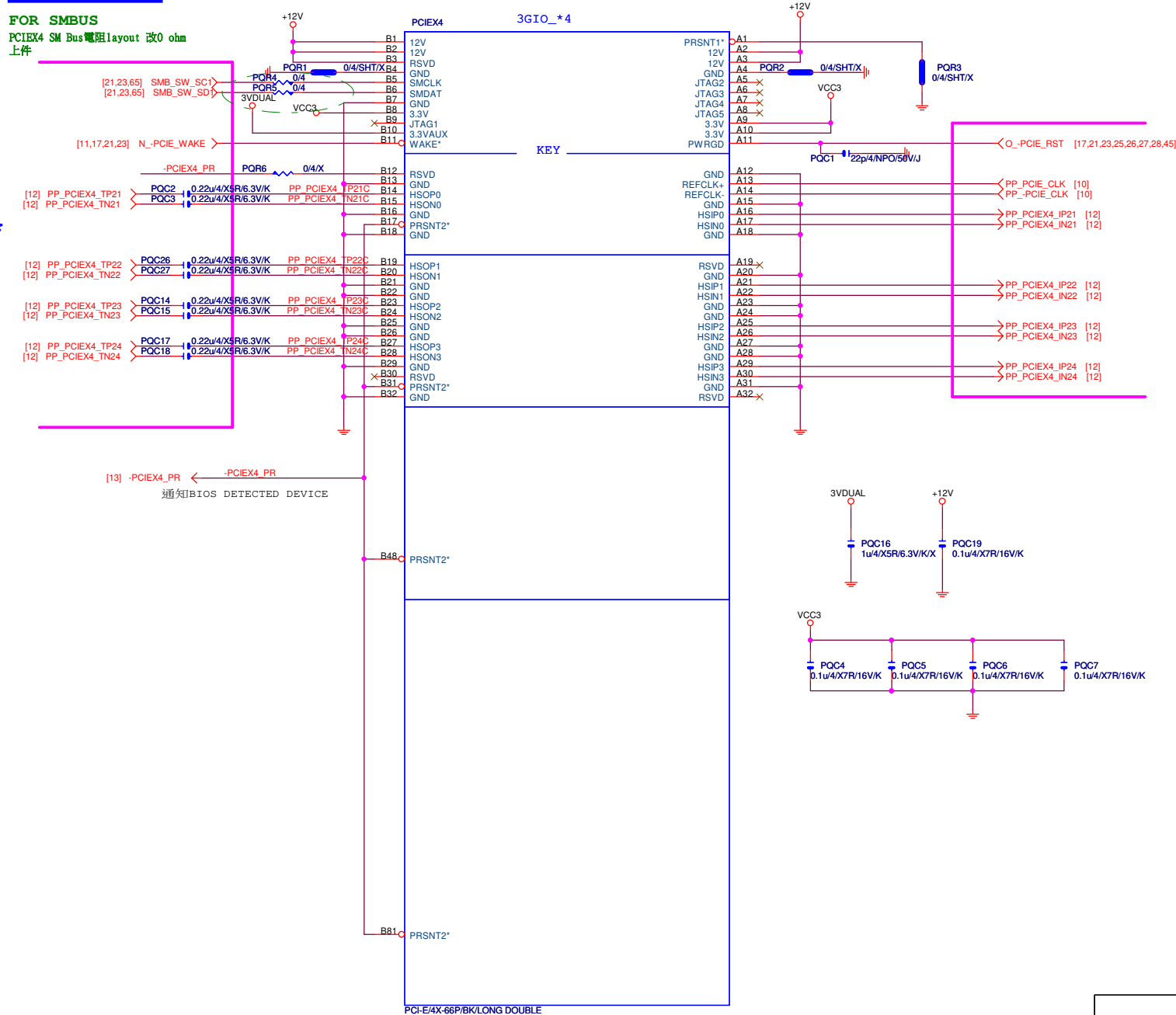
Rev 0.51

PCIE*4

★
Footprint "PCIESLOT-64P-1"

FOR SMBUS

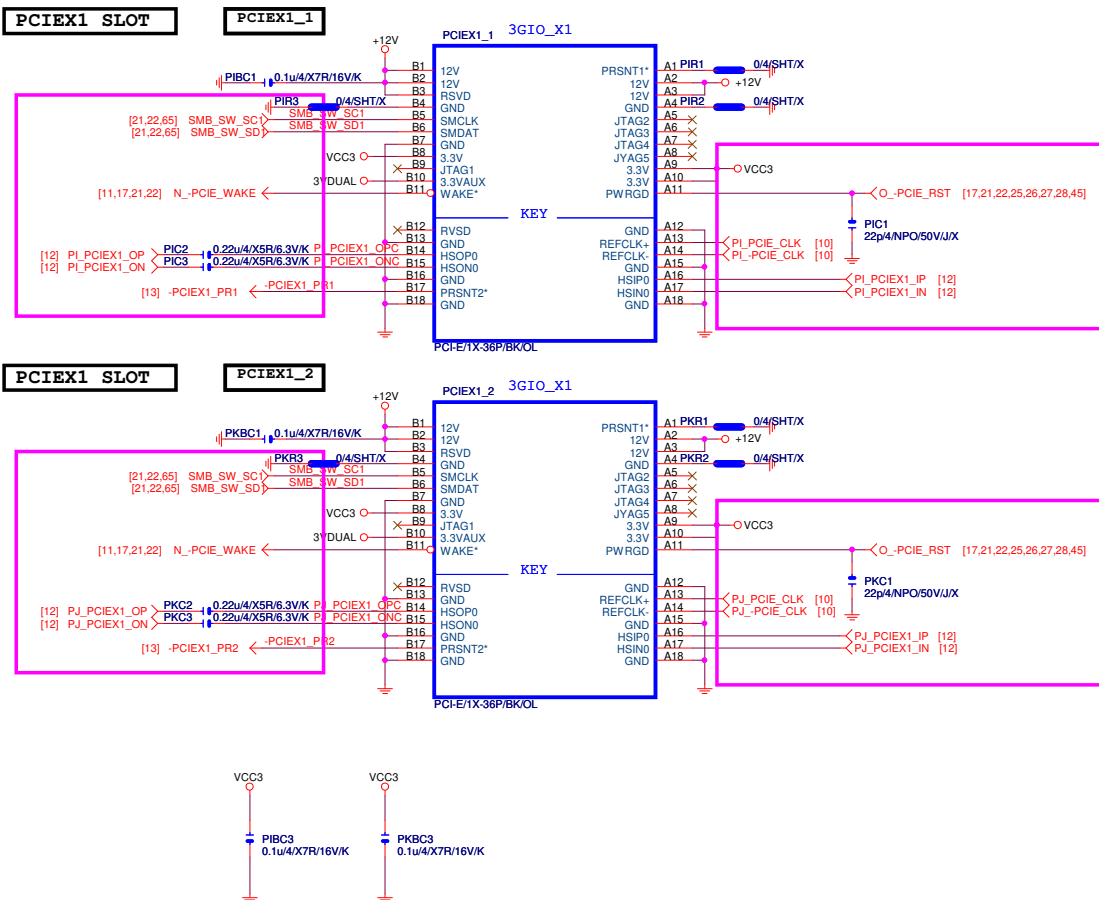
PCIE4 SM Bus電阻layout 改0 ohm
上件



黑色

Gigabyte Technology			
Title			
PCIE X4			
Size	Document Number		Rev
Custom	Z590 UD AC		1.0
Date:	Friday, December 11, 2020	Sheet	22 of 69

Rev 0.51



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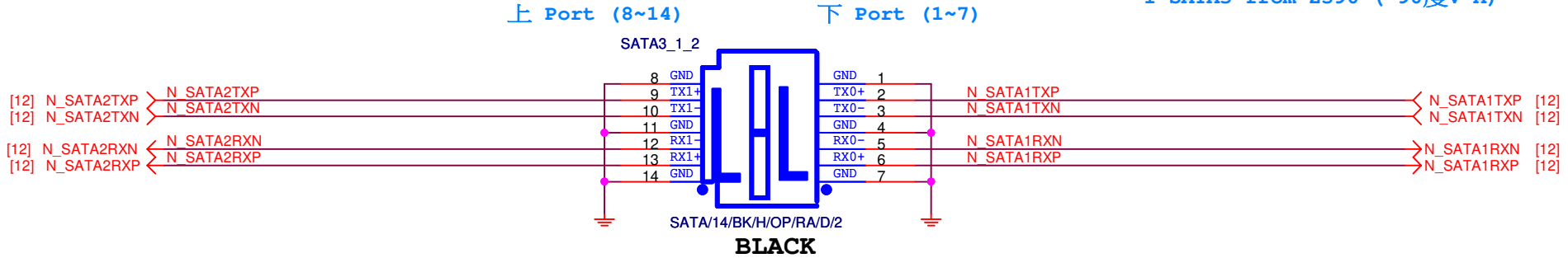
Gigabyte Technology			
Title			
PCIE X1 *3			
Size	Document Number	Rev	
Custom	Z590 UD AC	1.0	
Date:	Friday, December 11, 2020	Sheet	23 of 69

SATA3 1/2

IO19/IO20 To SATA3 port1/2

4 SATA3 from Z590 (180度R-A)

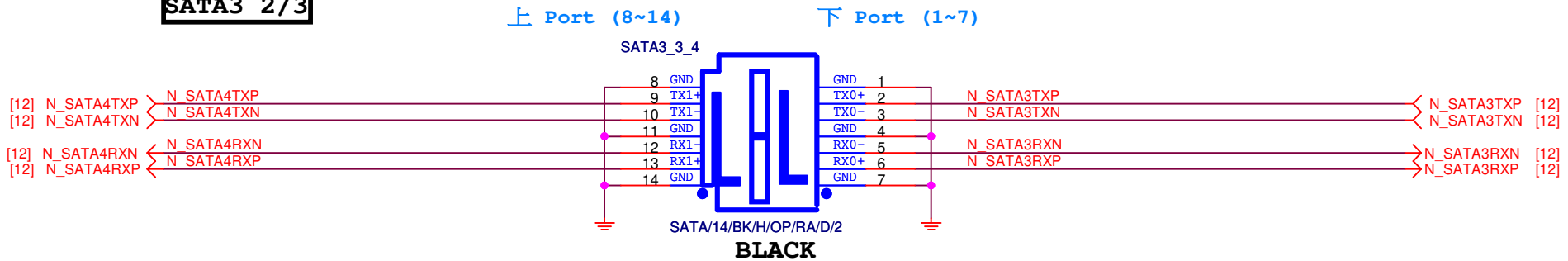
1 SATA3 from Z590 (90度V-A)



Footprint : H2X7-SATA2-D10

SATA3 2/3

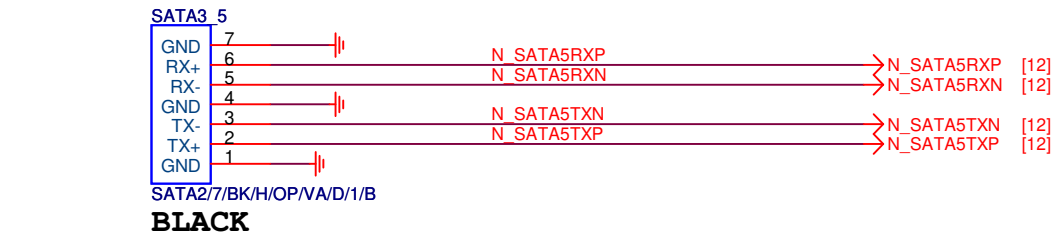
IO21/IO22 To SATA3 port3/4



Footprint : H2X7-SATA2-D10

SATA3 4/5

IO23 To SATA3 port5



Footprint : H1X7-SATA2-HS-MA5K

Gigabyte Technology

Title		
SATA		
Size	Document Number	Rev
Custom	Z590 UD AC	1.0
Date:	Friday, December 11, 2020	Sheet 24 of 69

Rev 0.1

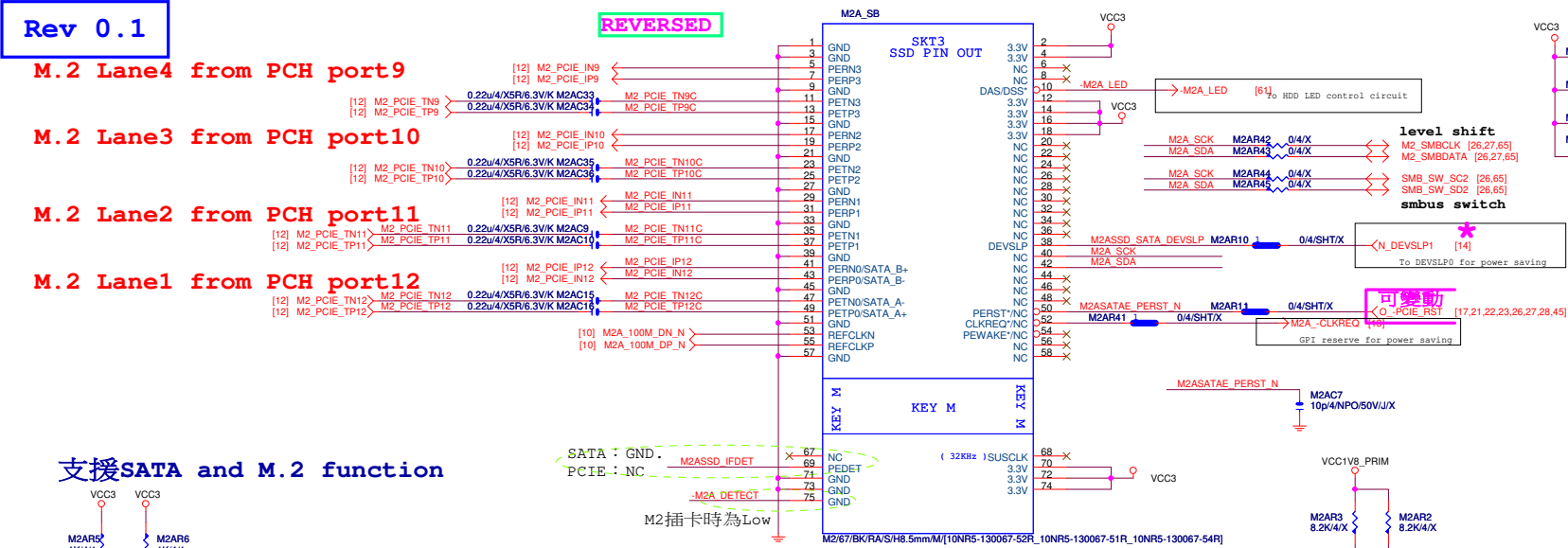
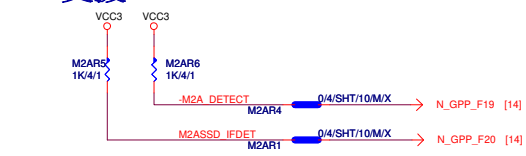
M.2 Lane4 from PCH port9

M.2 Lane3 from PCH port10

M.2 Lane2 from PCH port11

M.2 Lane1 from PCH port12

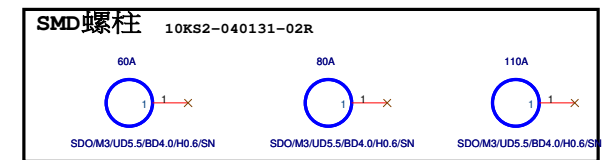
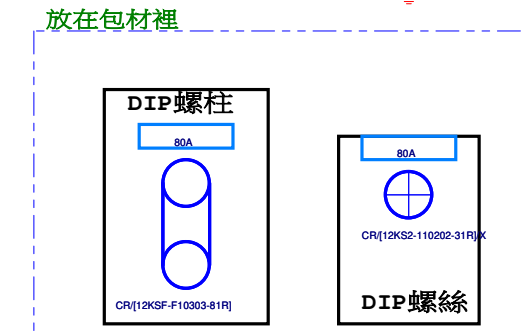
支援SATA and M.2 function



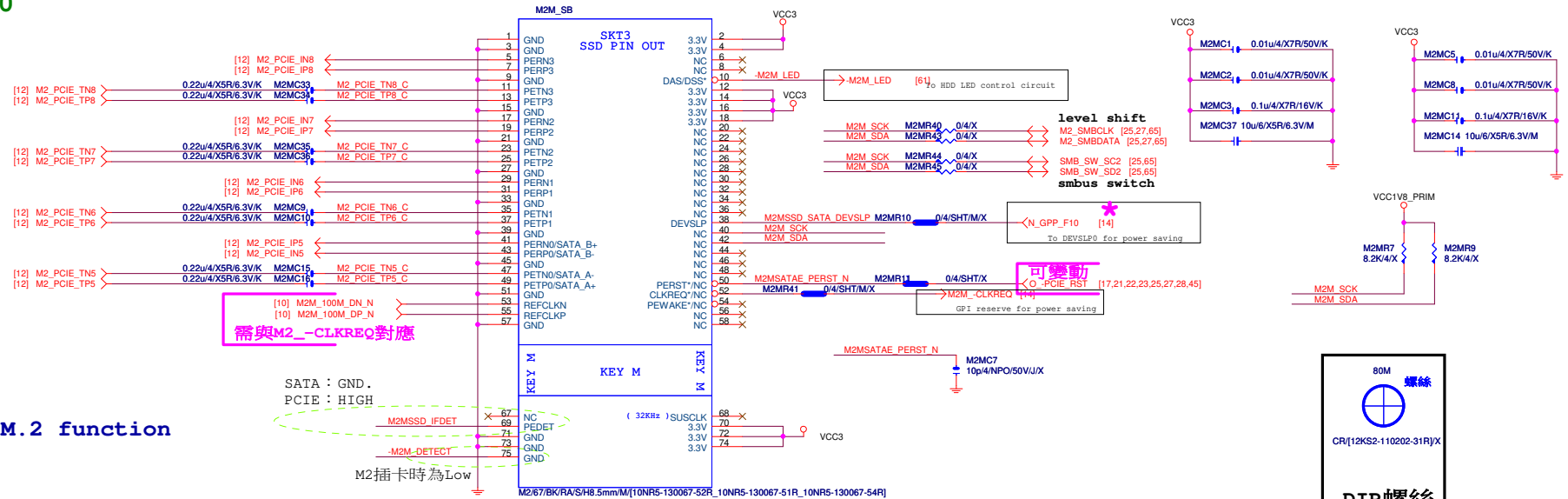


架高
Footprint : M2_110_H2MM8W

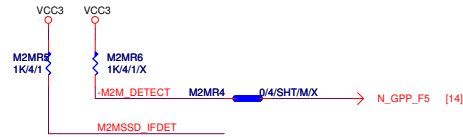
Flex IO priority	N_GPP_F20	IO14 PCIe#9	IO15 PCIe#10	IO16 PCIe#11	IO17 PCIe#12
M2A SATA	L	PCIe	PCIe	SATA 0	SATA 1
M2A PCIe (PCIe Reverse)	H	PCIe	PCIe	PCIe	PCIe



* Footprint : HOLE_C236D165-A
10KS2-040131-02R:SDO/M3/UD5.5/BD4.0/H0.6/SN



支援SATA and M.2 function

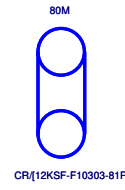


架高

Footprint : M2_110_H2MM8W

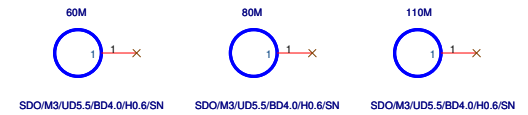
Flex IO priority	N_GPP_F5	IO22 PCIe#17	IO23 PCIe#18	IO24 PCIe#19	IO25 PCIe#20
M2M SATA	L	SATA 4	SATA 5	PCIE	PCIE
M2M PCIE	H	PCIE	PCIE	PCIE	PCIE

DIP螺柱



SMD螺柱

10KS2-040131-02R



Rev 0.1

M.2 Lane4 from CPU port4

M.2 Lane3 from CPU port3

M.2 Lane2 from CPU port2

M.2 Lane1 from CPU port1

支援SATA and M.2 function

需與M2_-CLKREQ對應

架高金屬加強
Footprint : M2_110_H2MM8W

DIP螺柱

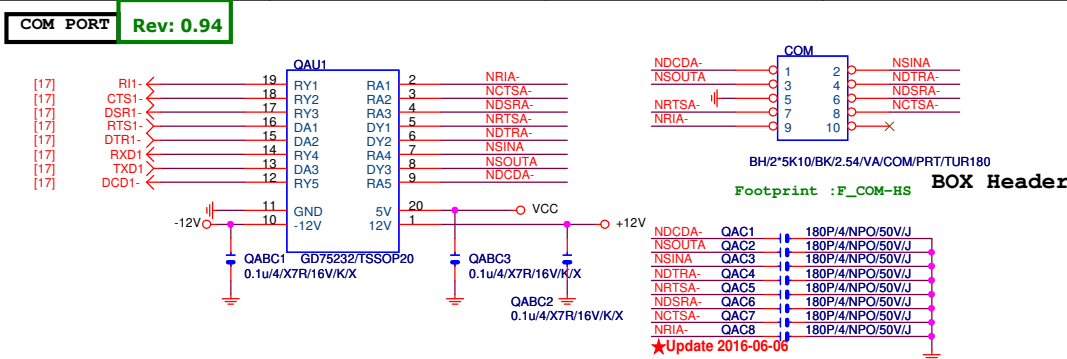
SMD螺柱

SMD螺柱

HS_DIP螺絲

Gigabyte Technology

Title			M.2 X4 (P)
Size	Document Number	Rev	
Custom	Z590 UD AC	1.0	
Date:	Friday, December 11, 2020	Sheet	27 of 69



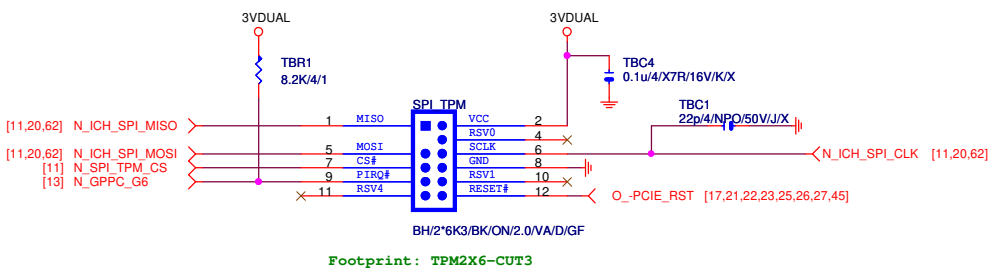
LPT PORT

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RTD3 GPIO refer by Intel RVP

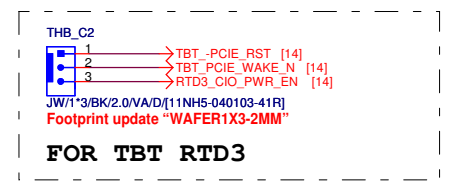
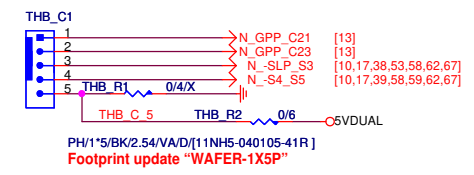
GPIO	CFL-S	CML-U	CML-H	CML-S
TBT_PERST_N	GPP_F_2	GPPC_C15_SLOT1_RST_N	GPP_F4_SATAPCIE7	GPP_F2
TBT_Wake_N	GPP_H_15	GPPC_D11_SLOT1_WAKE_N	GPPK_18	GPP_H15
RTD3_PWN_EN	GPP_I_5	GPPC_D15	GPP_H_16_SML4_CLK	GPP_K23

TPM CONNECT



Thunderbolt

★Update 2015-12-29



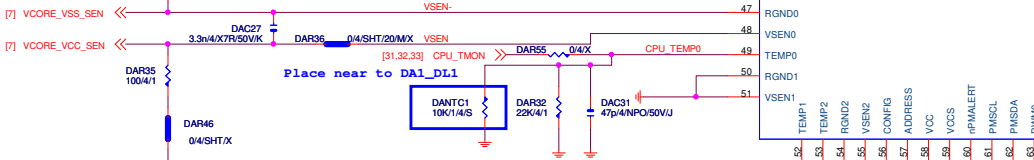
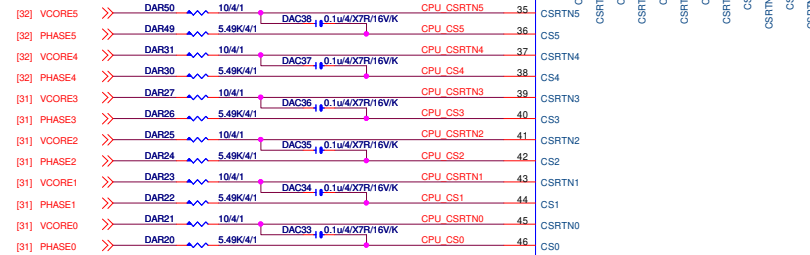
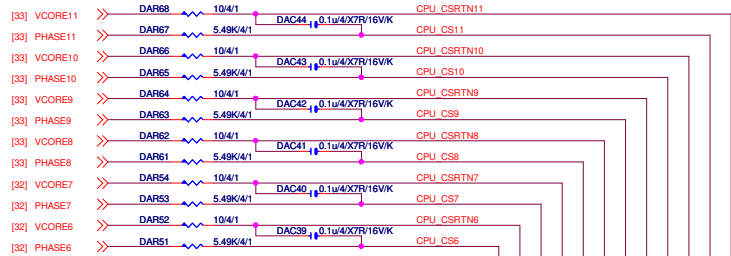
FOR TBT RTD3

Z490系列使用

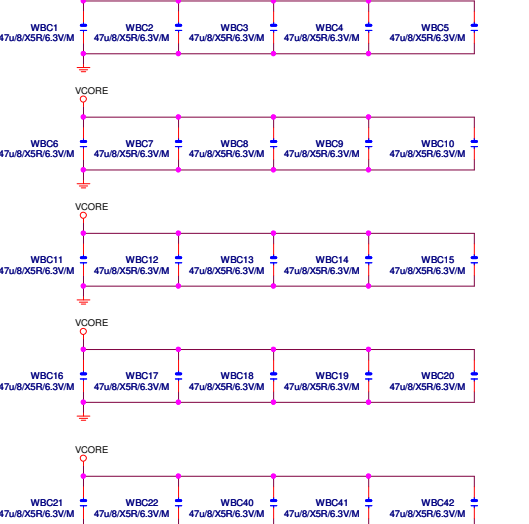
TBT_PCIE_RST : CFL connector to GPP_F_2
TBT_PCIE_WAKE_N : CFL connector to GPP_H_15
RTD3_CIO_PWR_EN : CFL connector to GPP_K_3

Gigabyte Technology		
Title		
FP,F_USB,USB PWR,BZ		
Size	Document Number	Rev
Custom	Z590 UD AC	1.0
Date:	Friday, December 11, 2020	Sheet 28 of 69

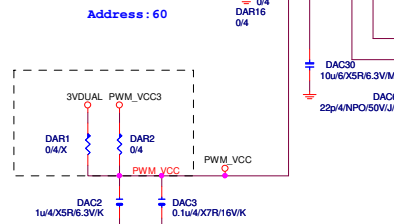
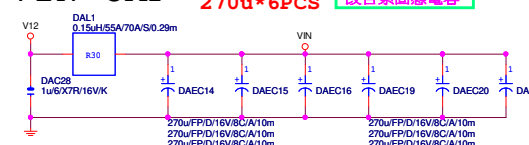
REV:0.1



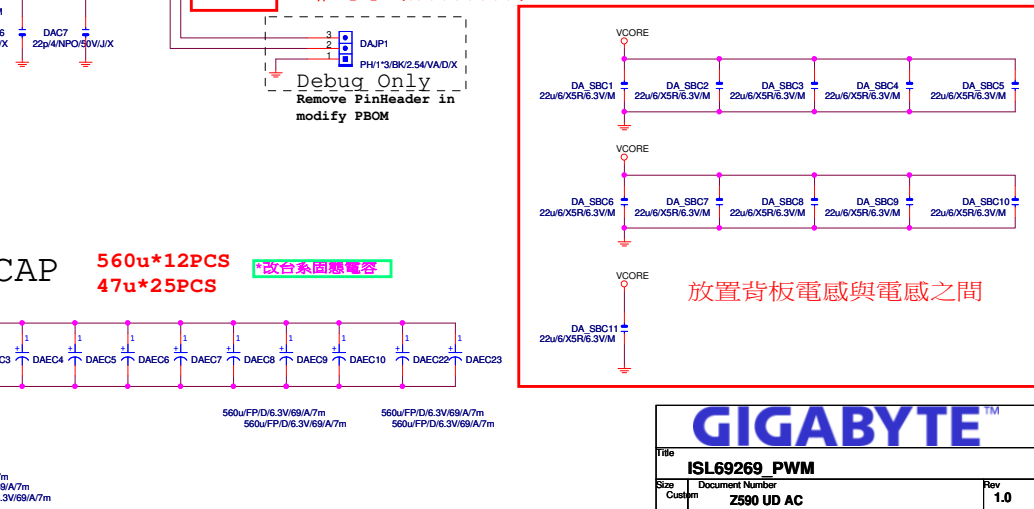
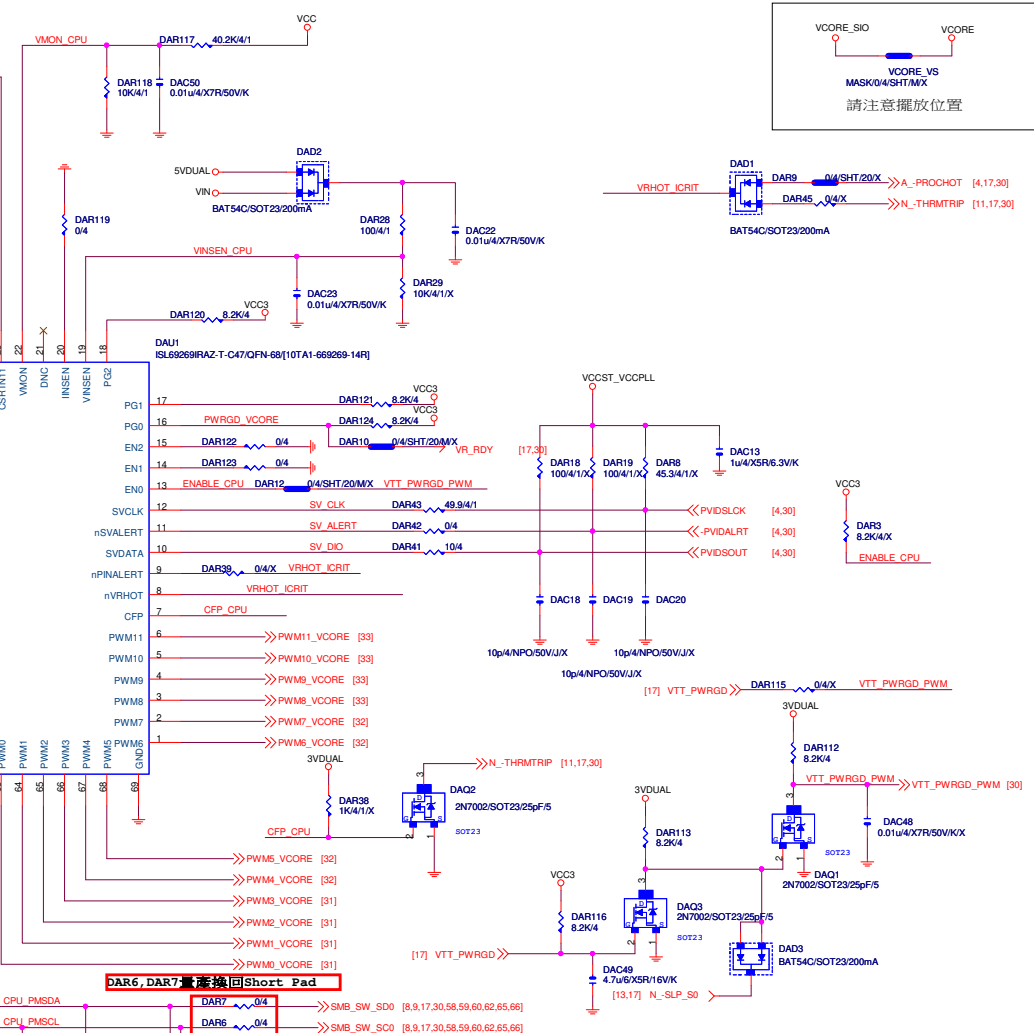
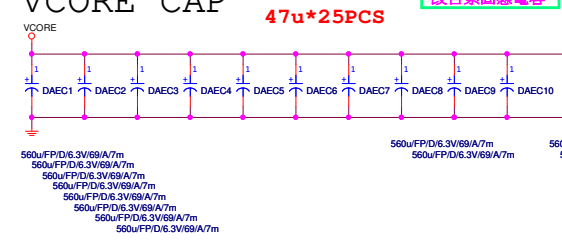
放CPU SOCKET (TOP LAYER)



VIN CAP 270u*6PCS 改台系固態電容

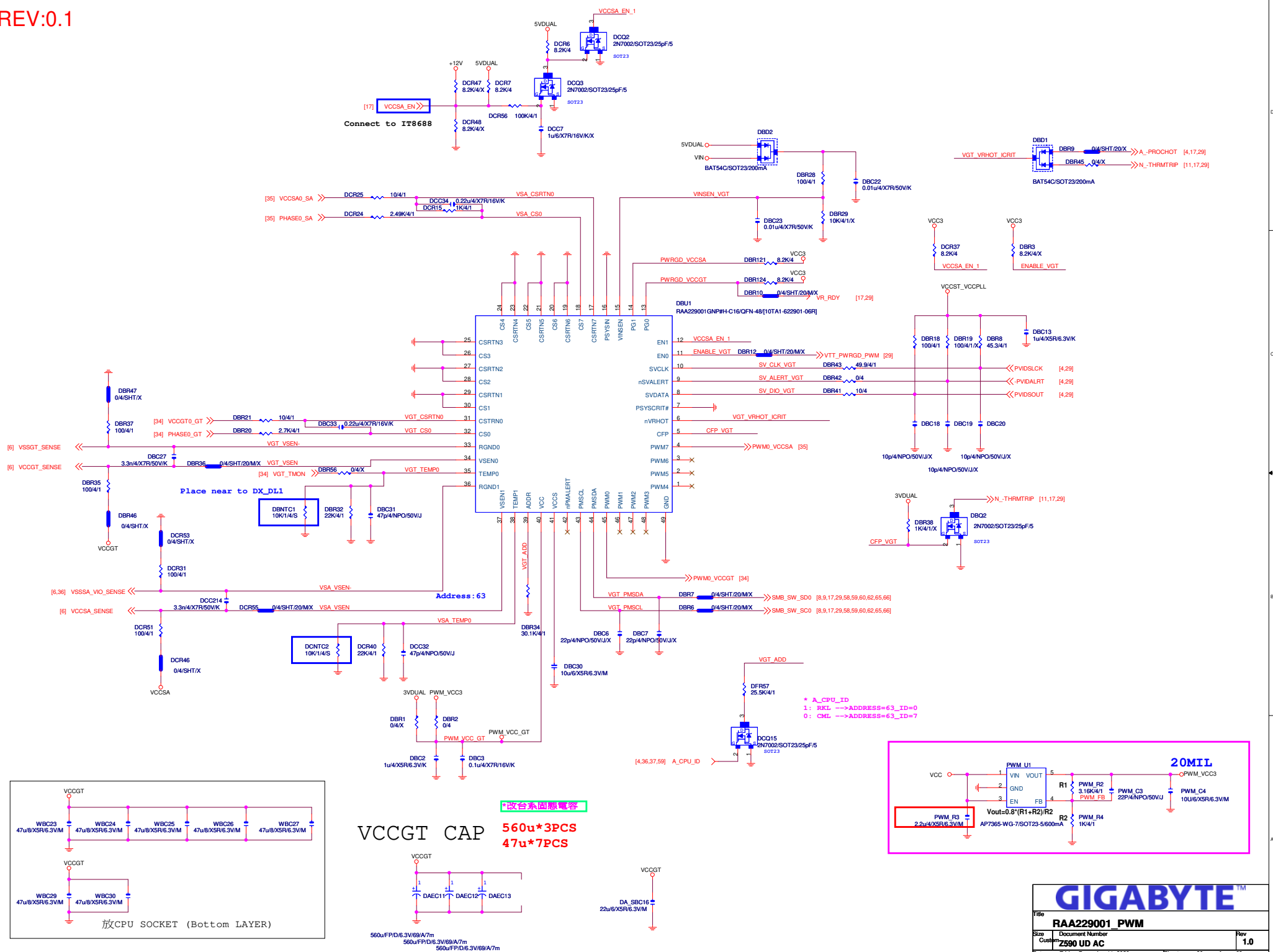


VCORE CAP 560u*12PCS 改台系固態電容

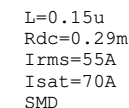
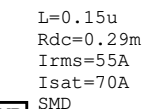
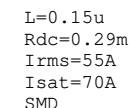
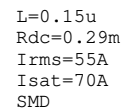


GIGABYTE

REV:0.1

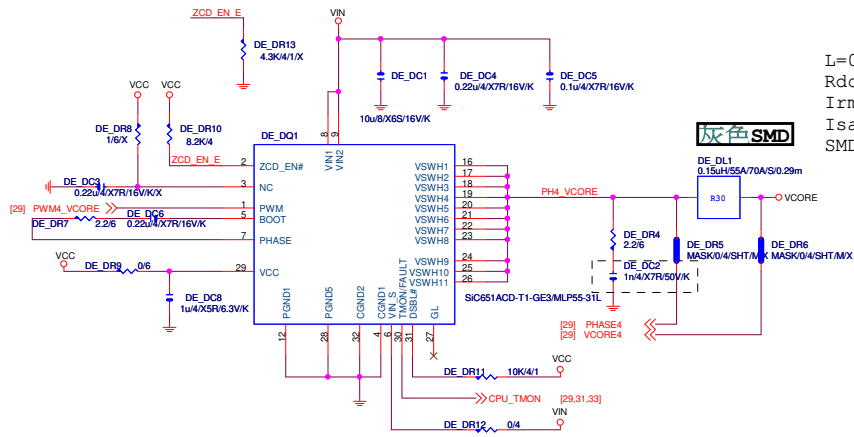


DRMOS使用NCP302155時PIN2 and PIN3要上件(Ex:DA_DR13.DA_DR8.DA_DC3)

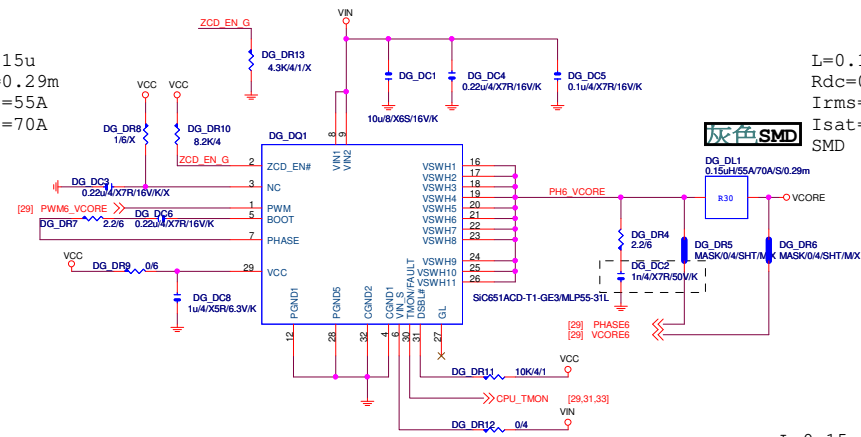


REV:0.1

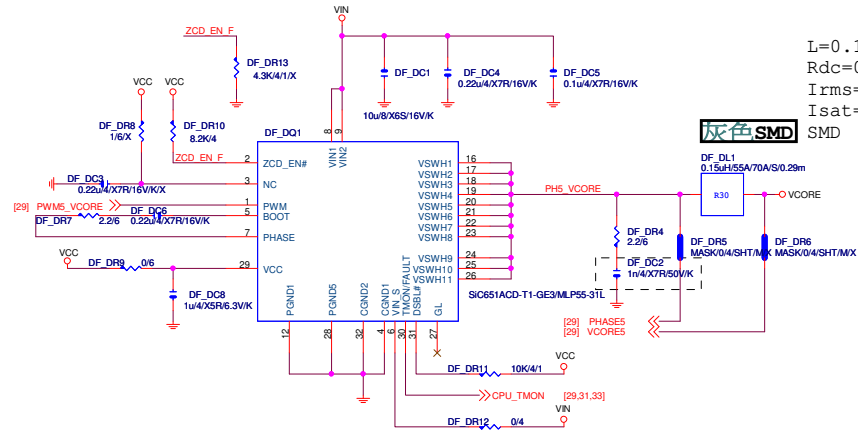
DRMOS使用NCP302155時PIN2 and PIN3要上件(Ex:DA_DR13.DA_DR8.DA_DC3)



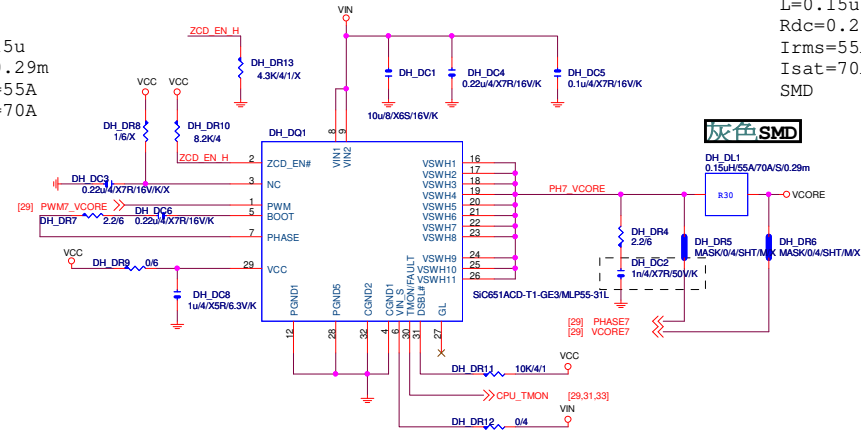
L=0.15u
Rdc=0.29m
Irms=55A
Isat=70A
SMD



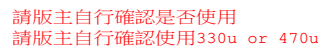
L=0.15u
Rdc=0.29m
Irms=55A
Isat=70A
SMD



L=0.15u
Rdc=0.29m
Irms=55A
Isat=70A
SMD



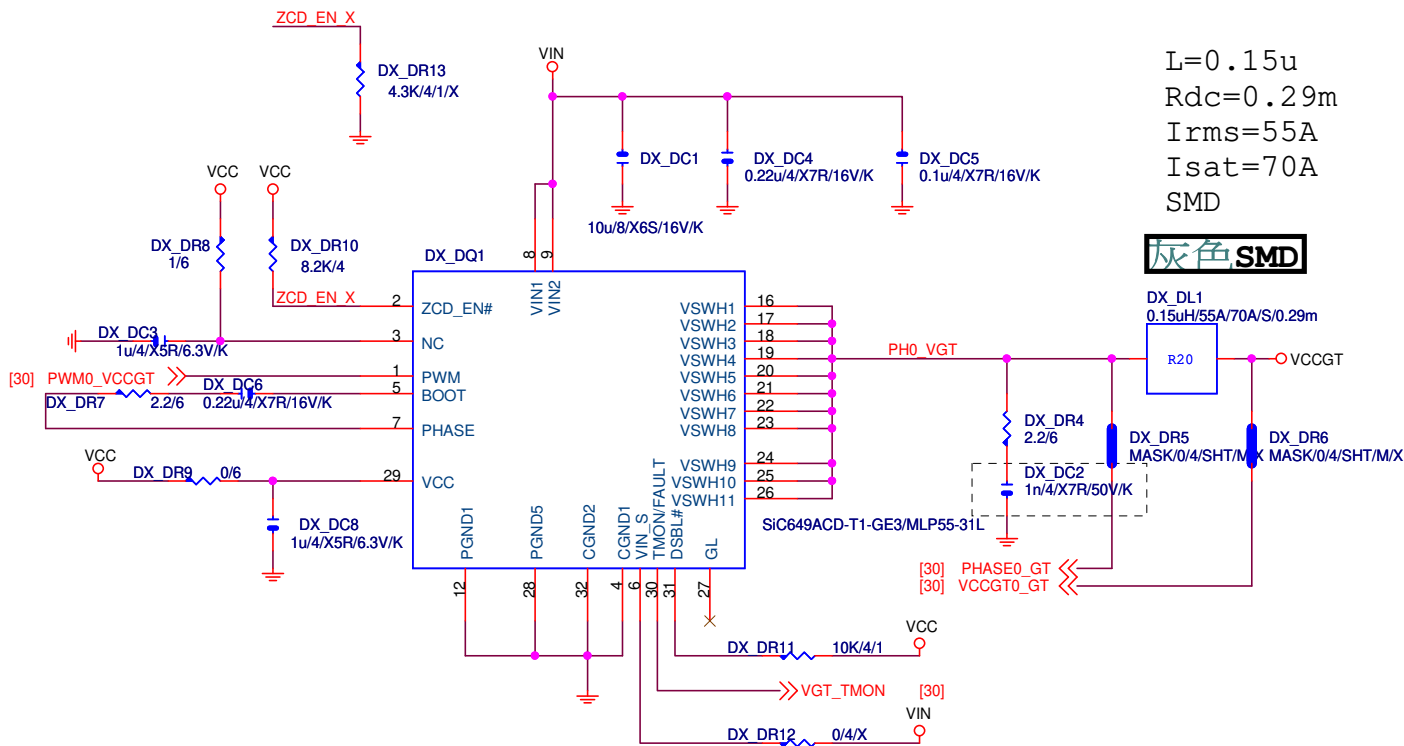
L=0.15u
Rdc=0.29m
Irms=55A
Isat=70A
SMD



請版主自行確認使用組態

REV:0.1

DRMOS使用NCP302155時PIN2 and PIN3要上件(Ex:DA_DR13.DA_DR8.DA_DC3)



GIGABYTE™

Title

VCCGT_DRMOS

Size

Document Number

Custom

2590 UD AC

Rev

1.0

Date:

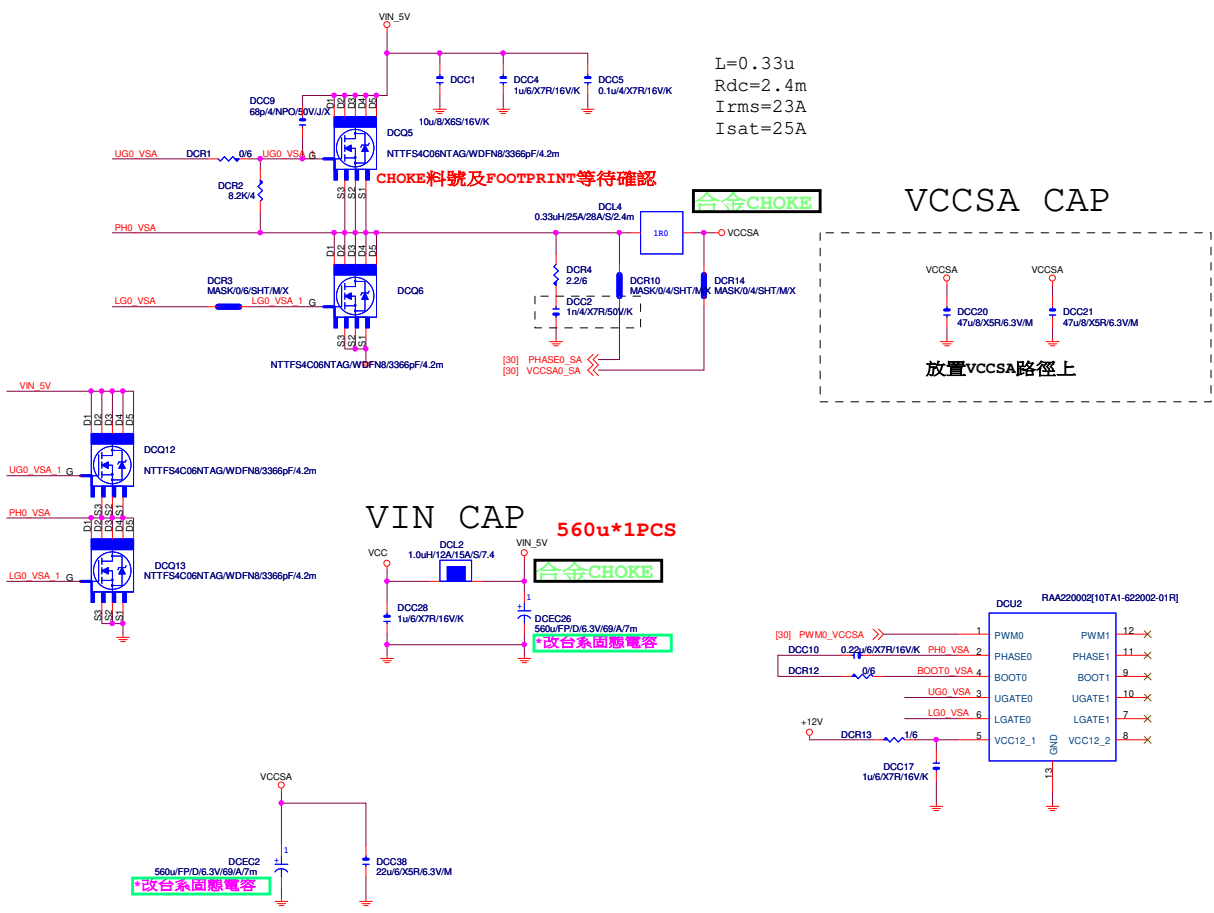
Friday, December 11, 2020

Sheet

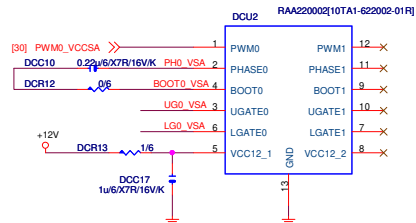
34

of

69



L=0.33u
Rdc=2.4m
Irms=23A
Isat=25A



VCCIO

REV:0.2

RKL MODIFY

VIO_VSA_RGND DFR35 0/4/X VSSA_VIO_SENSE [6,30]
請盡量靠近分支點

CHOKE與CAP料號可變

合金CHOKE

注意耐壓

合金CHOKE

使用GPIO超壓須移除

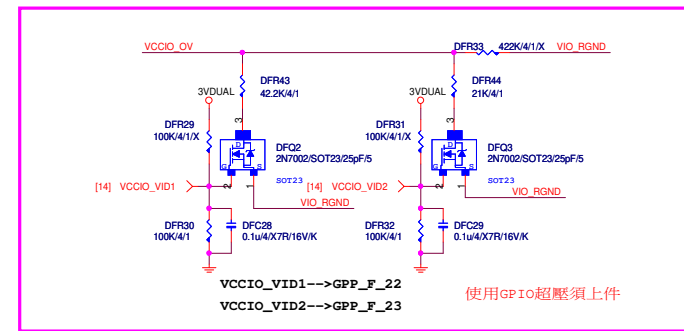
放CPU SOCKET (Bottom LAYER)

改台系固態電容

使用GPIO超壓須上件

使用GPIO超壓須上件

ADDRESS=2A VCCIO_OV
VREF=02

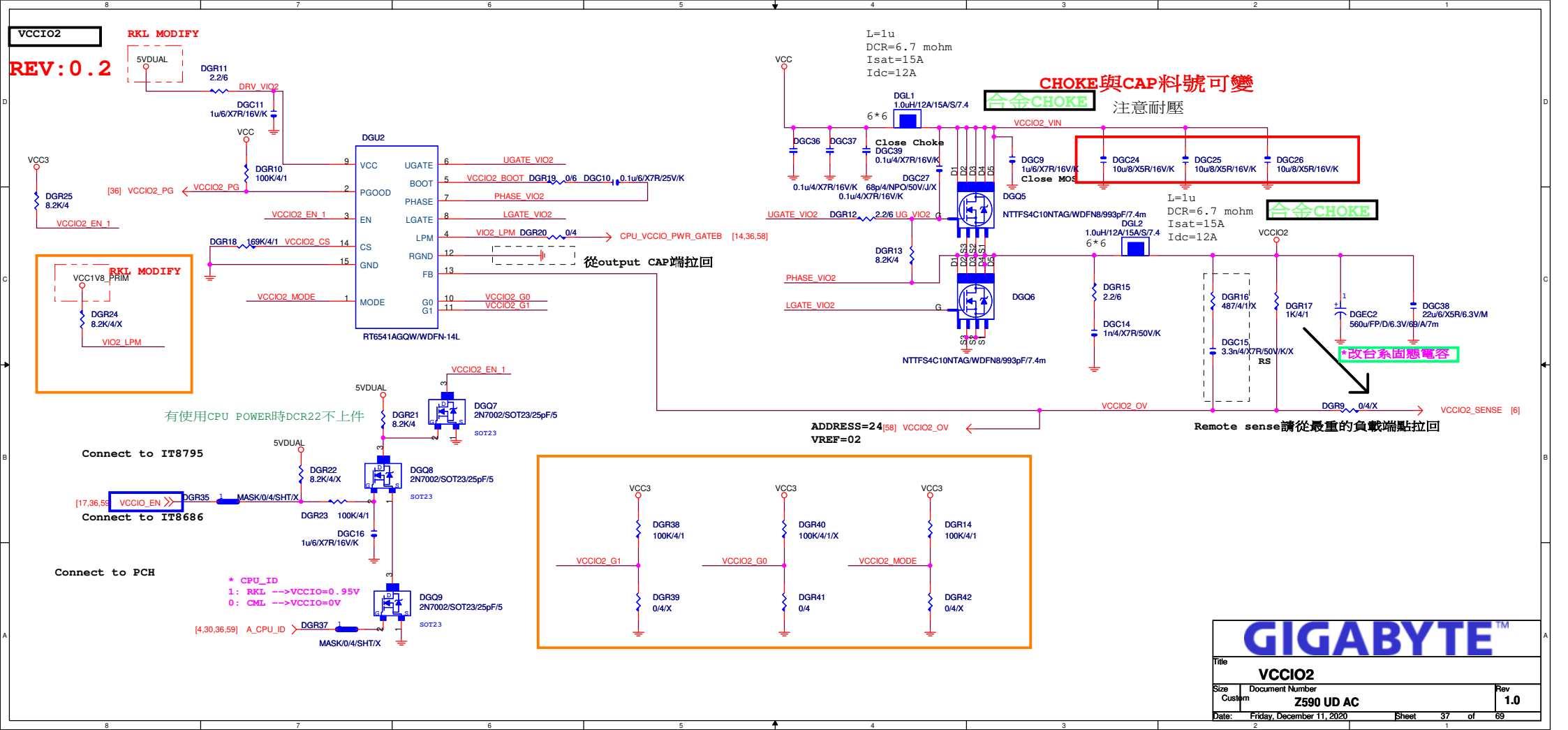


VCCIO_VID1	VCCIO_VID2	VCCIO_O_G1	VOUT
LOW	LOW	LOW	0.950V
LOW	LOW	HIGH	1.050V
HIGH	LOW	HIGH	1.075V
LOW	HIGH	HIGH	1.100V
HIGH	HIGH	HIGH	1.125V

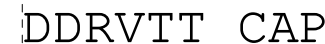
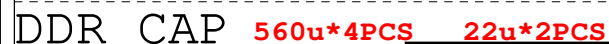
Mode	VR	Mode logic	LPM	VID Setting G1 logic	G0 logic	Vout (V)
Mode1	VCCIO	0	0	x	x	0(LPM)
			1	0	0	0.85
			1	0	1	0.875
			1	1	0	0.95
			1	1	1	0.975
Mode2	VPRIMCORE	Floating	0	x	x	0.7V(LPM)
			1	0	0	0.85
			1	0	1	0.9
			1	1	0	0.95
			1	1	1	1
Mode3	VccEDRAM/ VccEOPIO	1	0	x	x	0(LPM)
			1	0	0	0.8
			1	0	1	0.95
			1	1	0	1
			1	1	1	1.05

GIGABYTE™

Title		VCCIO	
Size	Document Number	Z590 UD AC	
Custom			Rev 1.0
Date:	Friday, December 11, 2020	Sheet	36 of 69



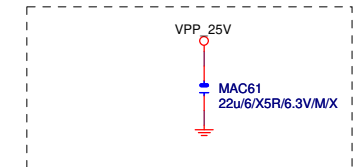
DDR4



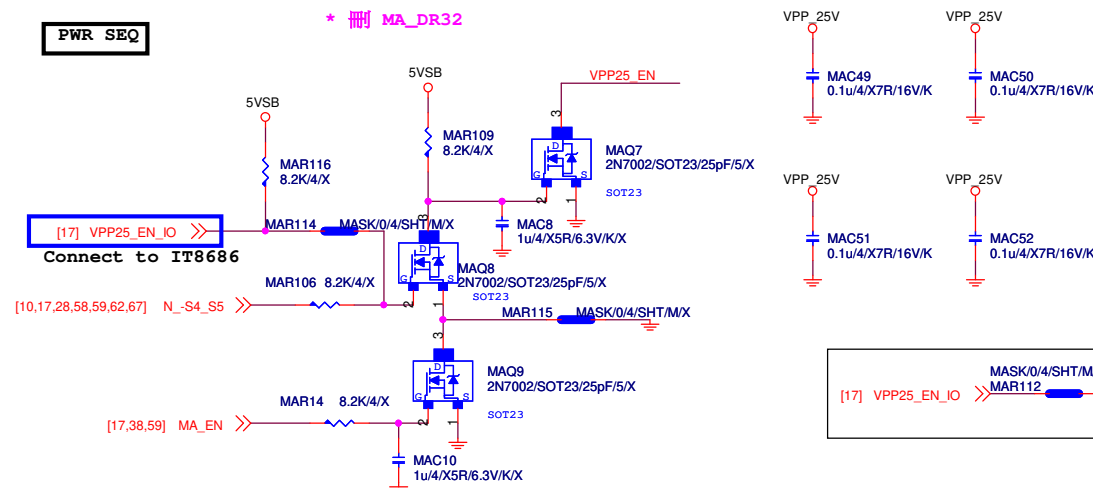
Title			
RT8120_DDR4 POWER			
Size	Document Number	Rev	
Custom	Z590 UD AC	1.0	
Date:	Friday, December 11, 2020	Sheet	38 of 69

VPP 25V

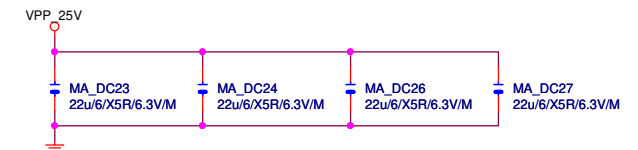
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請放置CHOKE一出來位置.先預留.
請自行確認ripple後再決定是否上件



VPP CAP 22u*4PCS

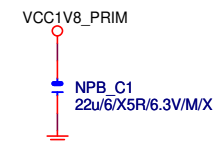
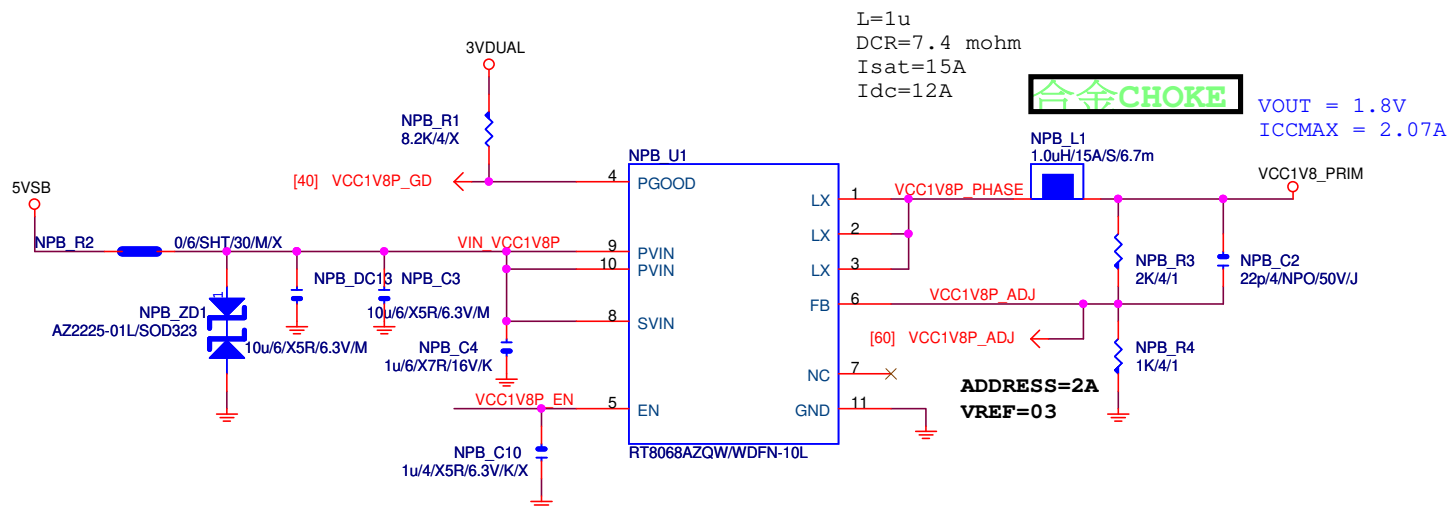
**GIGABYTE™**

Title			
RT8068_VPP25 POWER			
Size	Document Number	Rev	
Custom	Z590 UD AC	1.0	
Date:	Friday, December 11, 2020	Sheet	39 of 69

REV: 0.1

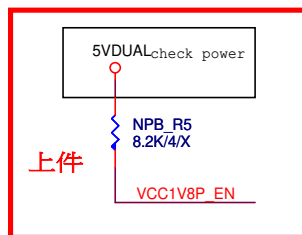
VCC1V8 PRIM

CHOKE與CAP料號可變



請放置CHOKE一出來位置.先預留.
請自行確認ripple後再決定是否上件

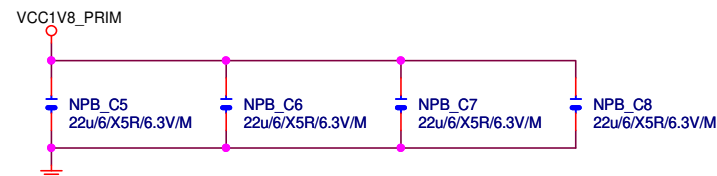
PWR SEQ



connect to PCH pin AD46



VCC1V8_PRIM CAP 22u*4PCS



GIGABYTE™

Title
RT8068_VCC1V8_PRIM

Size Document Number
Custom **Z590 UD AC**

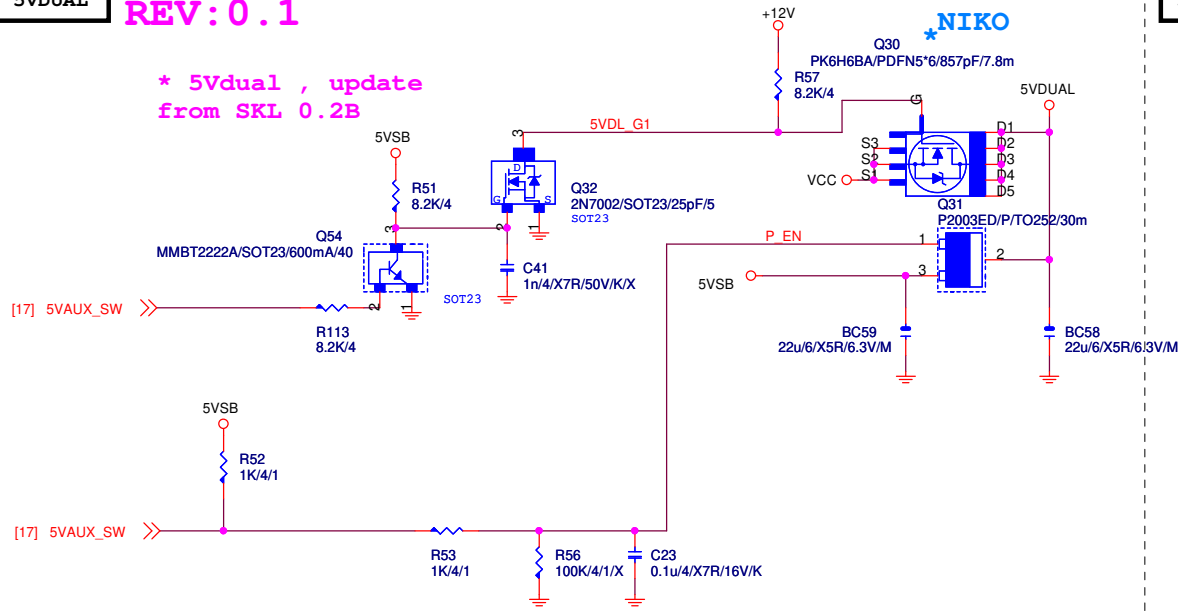
Rev
1.0

Date: Friday, December 11, 2020 Sheet 41 of 69

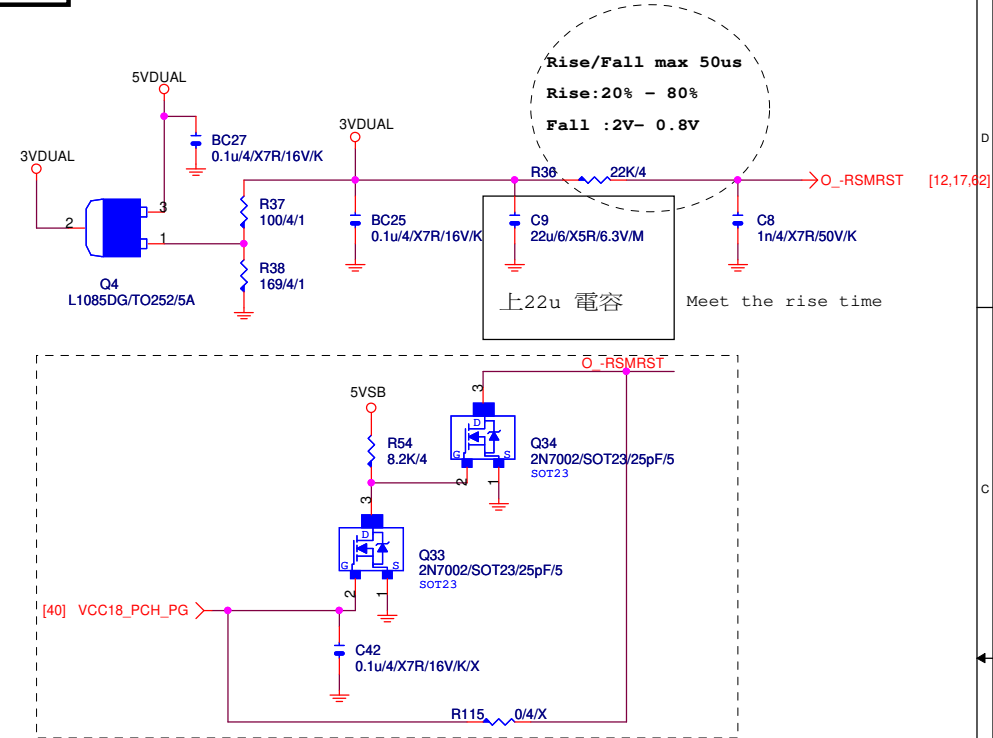
5VDUAL

REV:0.1

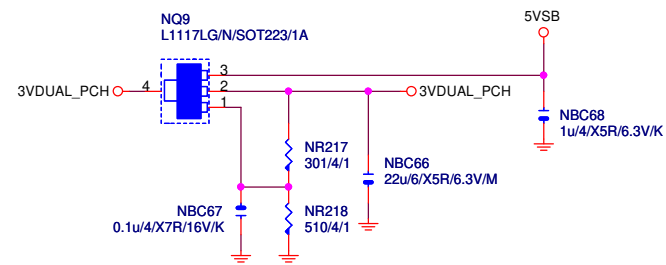
* 5Vdual , update
from SKL 0.2B



3VDUAL



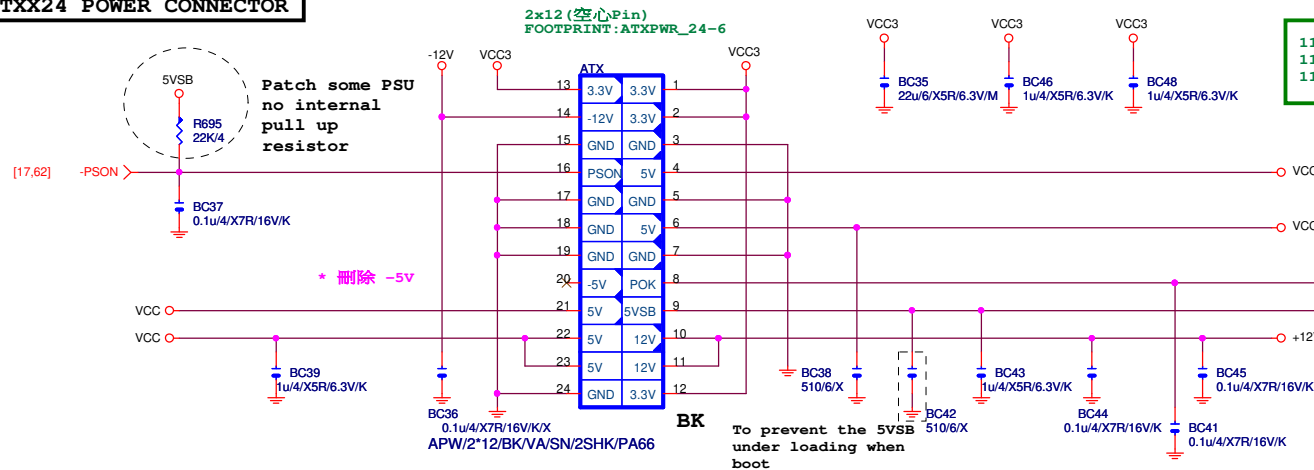
3VDUAL_PCH



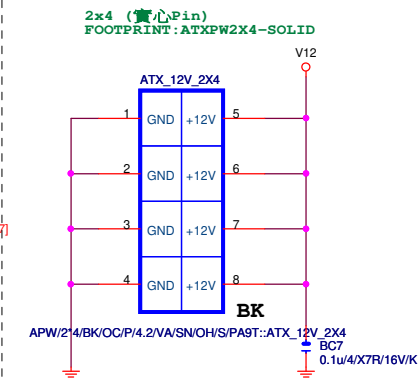
Gigabyte Technology

Title			
DISCRETE POWER			
Size	Document Number	Rev	
Custom		Z590 UD AC	
Date:		Friday, December 11, 2020	Sheet 42 of 69

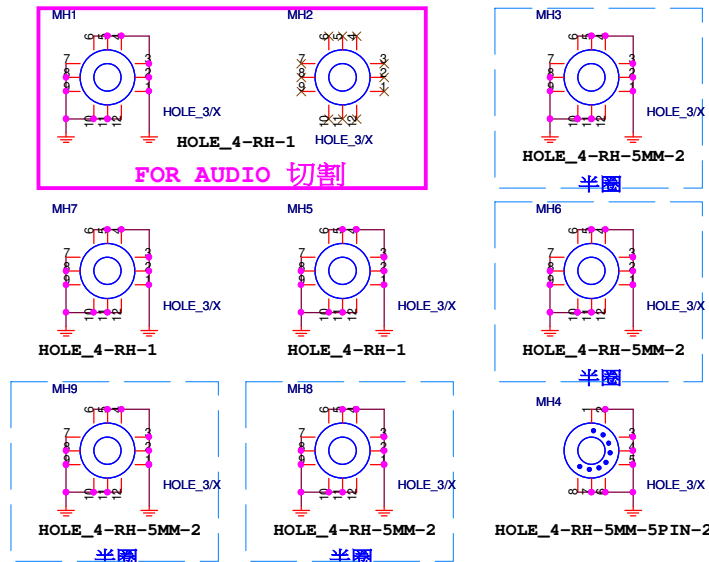
ATXX24 POWER CONNECTOR



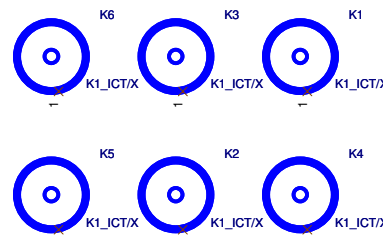
ATXX4 POWER CONNECTOR



螺絲孔

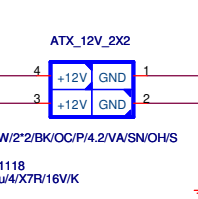
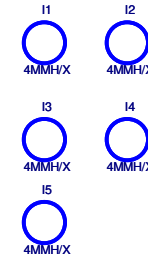


固定孔/光學點



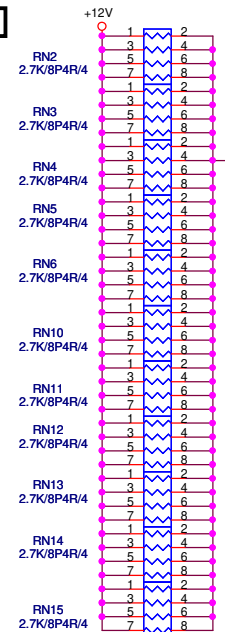
K1-ICT

To prevent the 5VSB
under loading when
boot

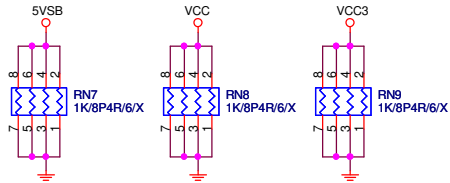


+12V DUMMY LOAD

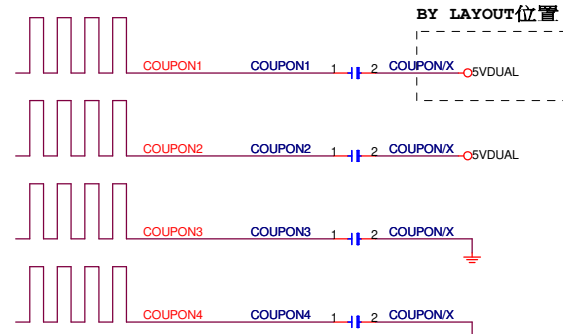
To fix 12V light load
abnormal issue



DUMMY LOAD



COUPON



Gigabyte Technology

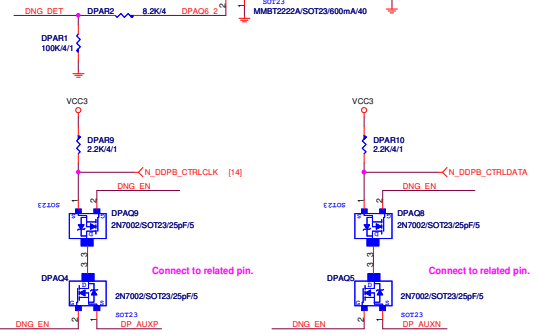
Title
ATX POWER CONNECTOR

Size Custom Document Number
Z590 UD AC

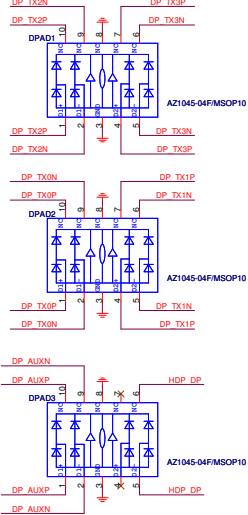
Date: Friday, December 11, 2020 Sheet 43 of 69

Rev 1.0

DNG_DET Hi=HDMI output,
Low=DP output.

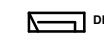
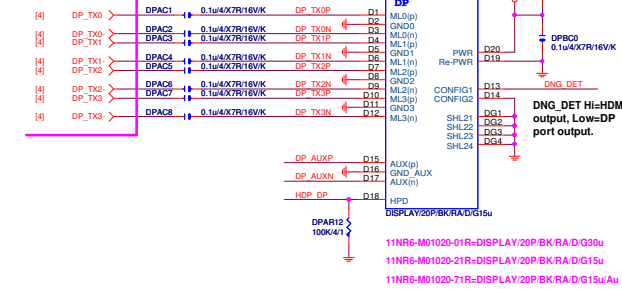


Close to connector



SINGLE Display Port

NET FROM CPU 可變



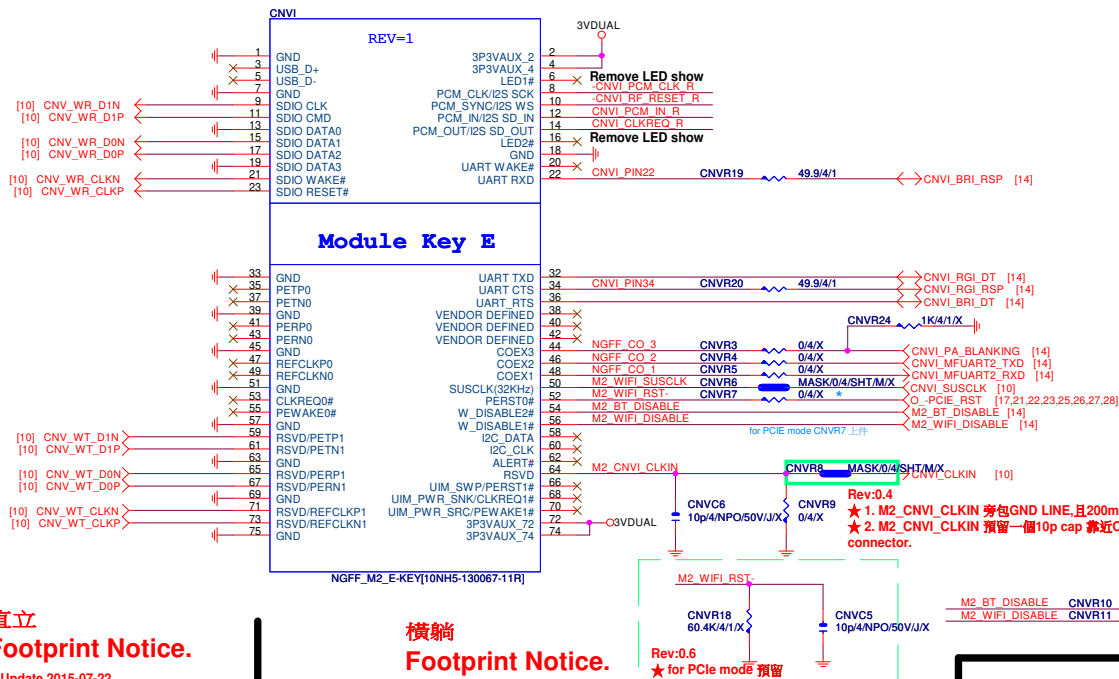
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Rev: 0.94

CNVi M2 WIFI

*全部上件

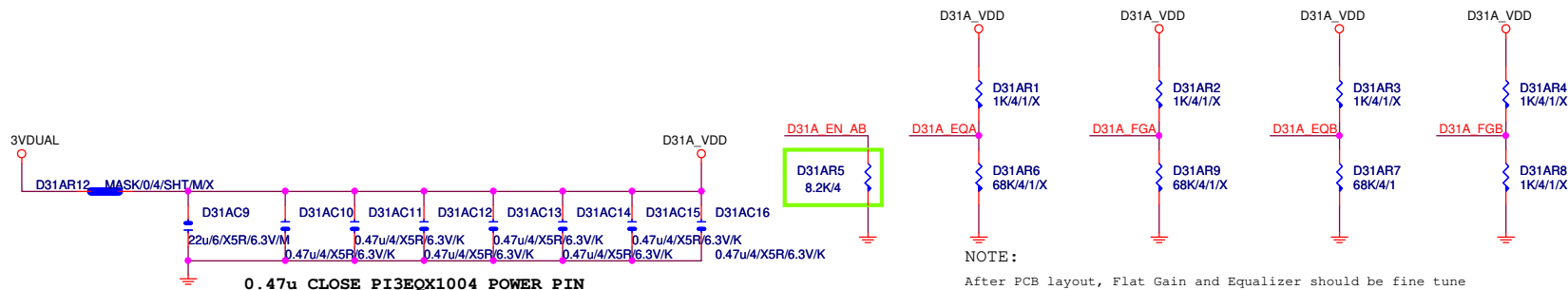
不支援PCIE介面WIFI及USB介面BT



USB3.2 GEN2 PI3EQX1004E Rev0.1

Type-A

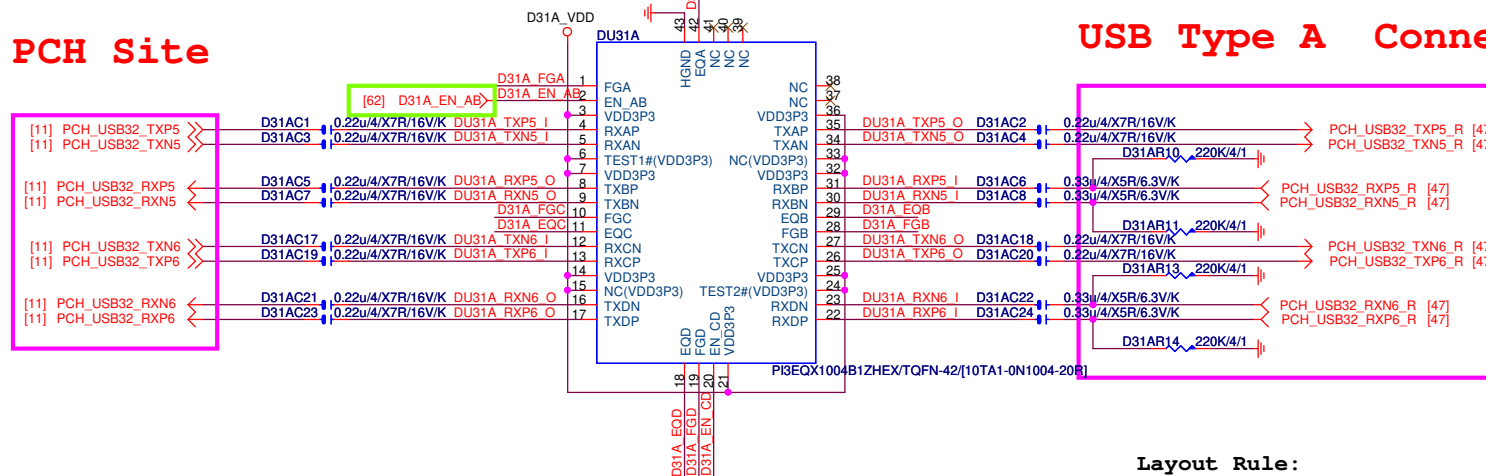
GROUP A



PCH Site

USB Type A Connector Site

可變

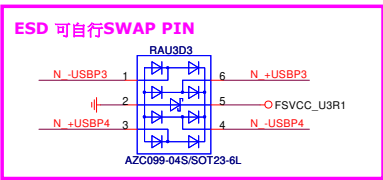


Layout Rule:

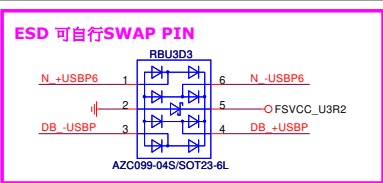
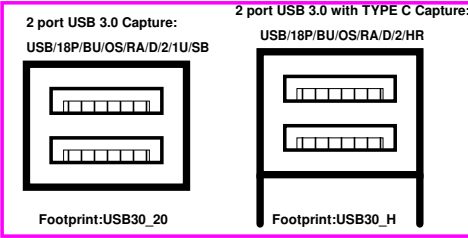
1. Differential Pair can't be swaped
2. Redriver to Connector Length min. 1 inch
3. PCH to Redriver Length min. 6 inch

GIGABYTE™

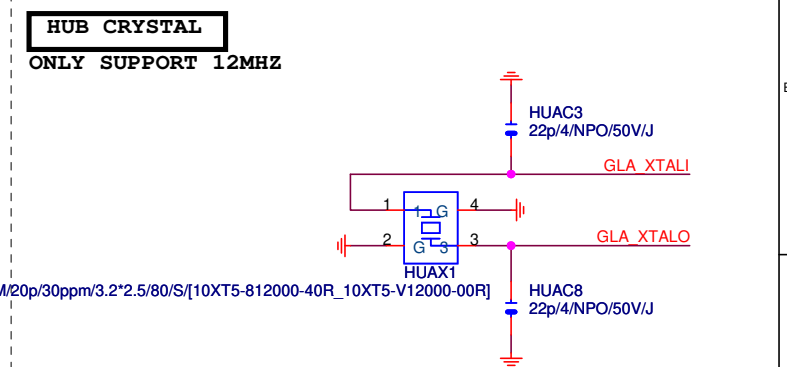
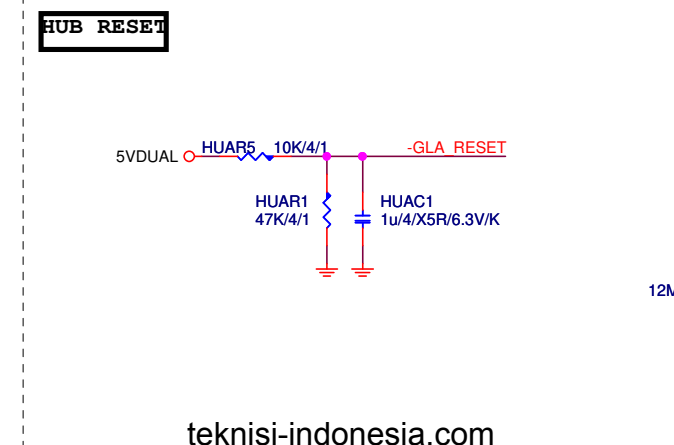
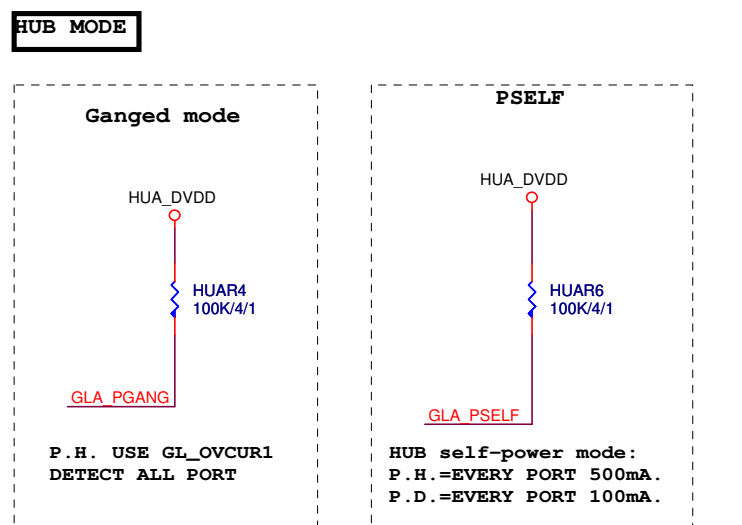
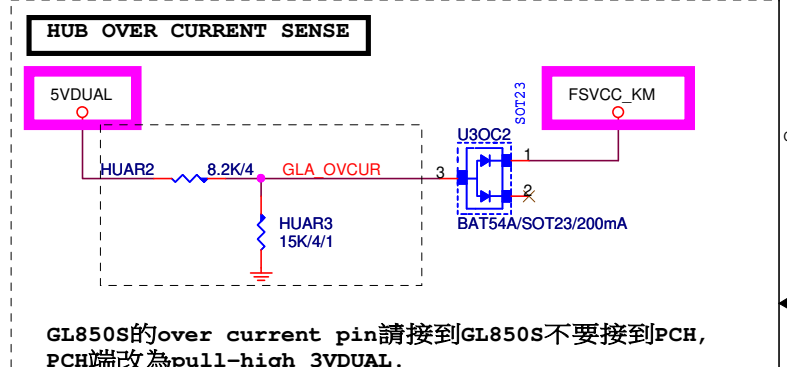
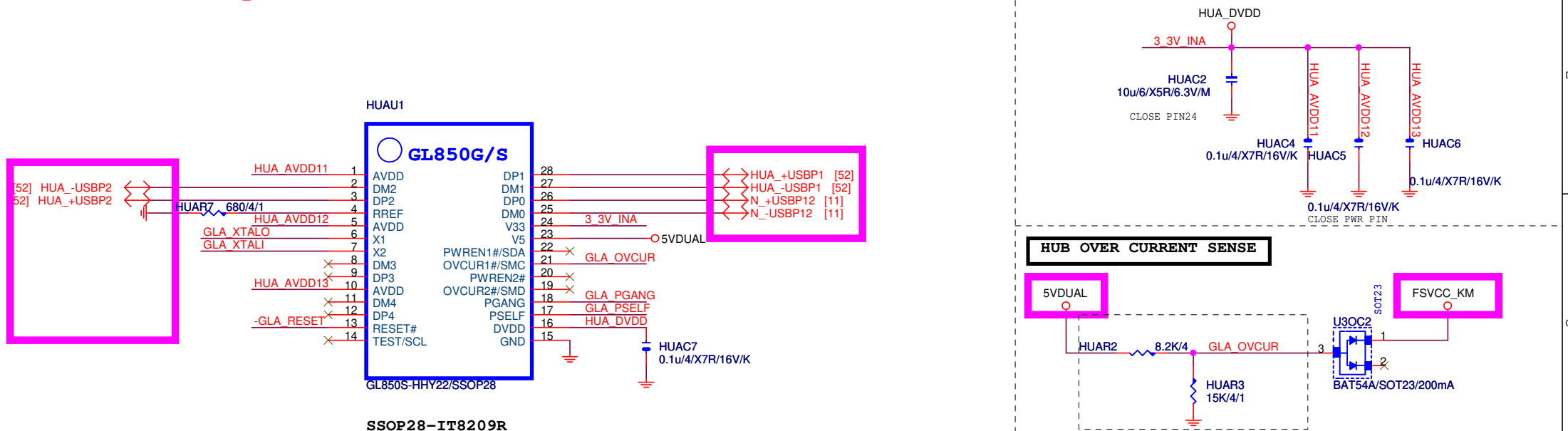
Title		
Redriver_A_Type-A		
Size B	Document Number	Rev
	Z590 UD AC	1.0
Date:	Friday, December 11, 2020	Sheet 46 of 69



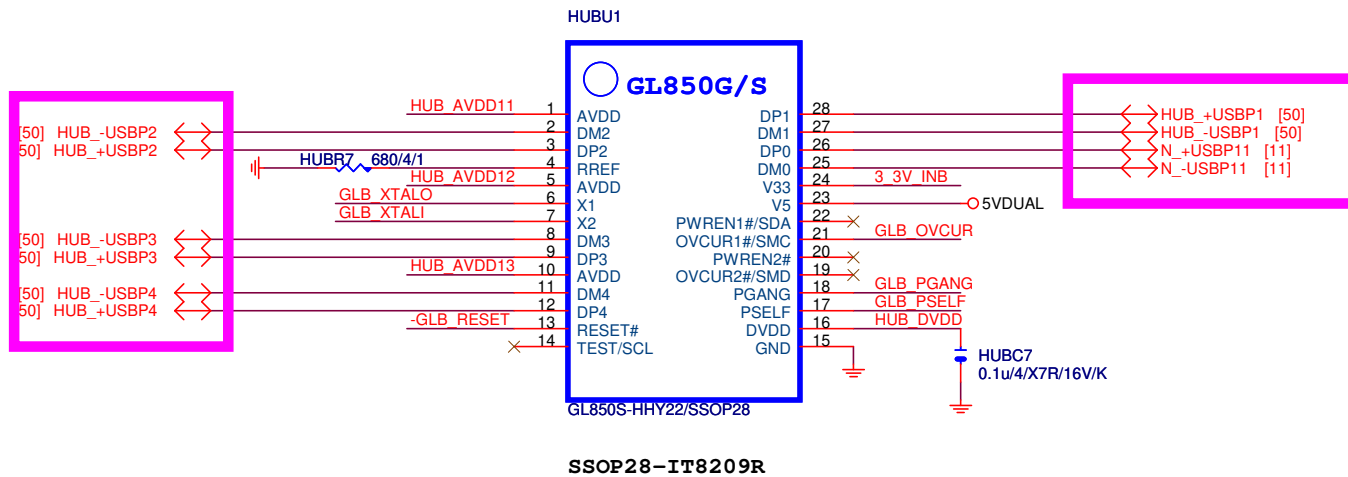
2 port USB 3.0 Capture:	2 port USB 3.0 with TYPE C Capture:
-------------------------	-------------------------------------



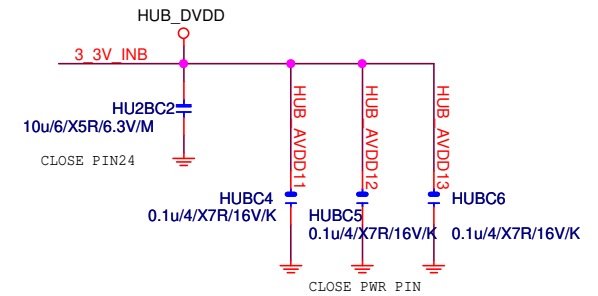
KB_MS_U32



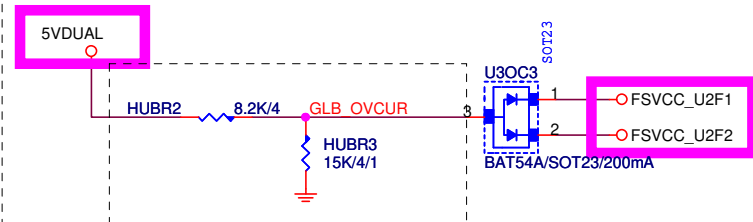
Dual USB2 HUB used Rev 0.1



HUB PWR

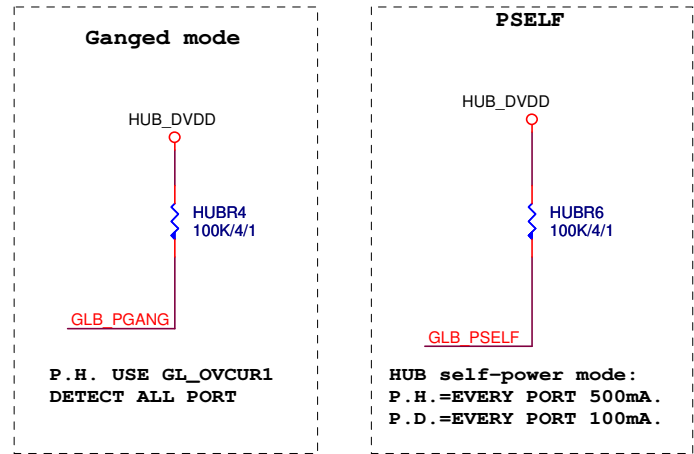


HUB OVER CURRENT SENSE

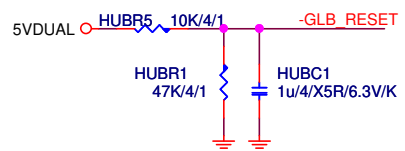


GL850S的over current pin請接到GL850S不要接到PCH, PCH端改為pull-high 3VDUAL.

HUB MODE

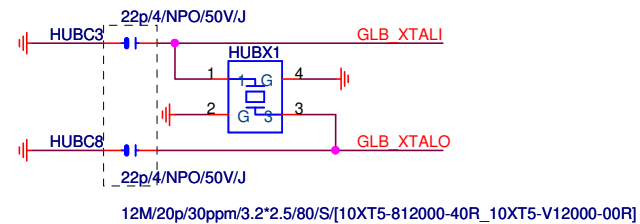


HUB RESET



HUB CRYSTAL

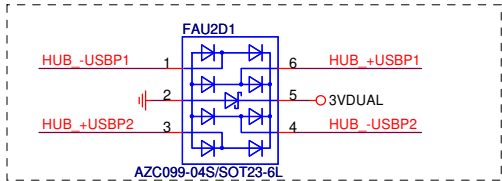
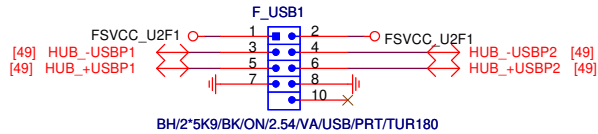
ONLY SUPPORT 12MHZ



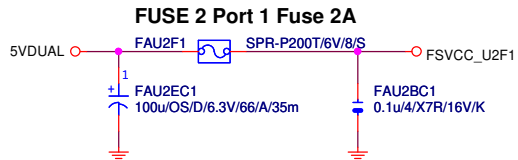
Gigabyte Technology			
Title			
HUB GL850GS_2			
Size	Document Number	Z590 UD AC	Rev
Custom			1.0
Date:	Friday, December 11, 2020	Sheet	49 of 69

FRONT USB1

NET 可變

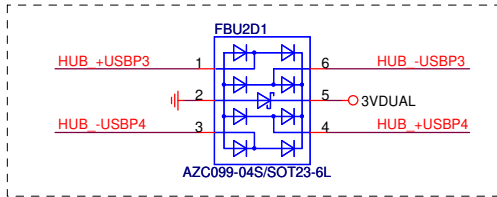
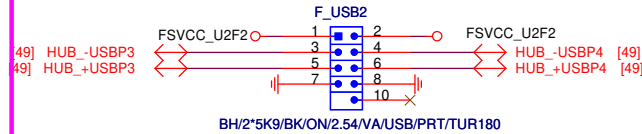


Close to connector
FUSE 2 Port 1 Fuse 2A

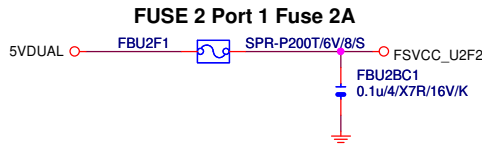


FRONT USB2

NET 可變

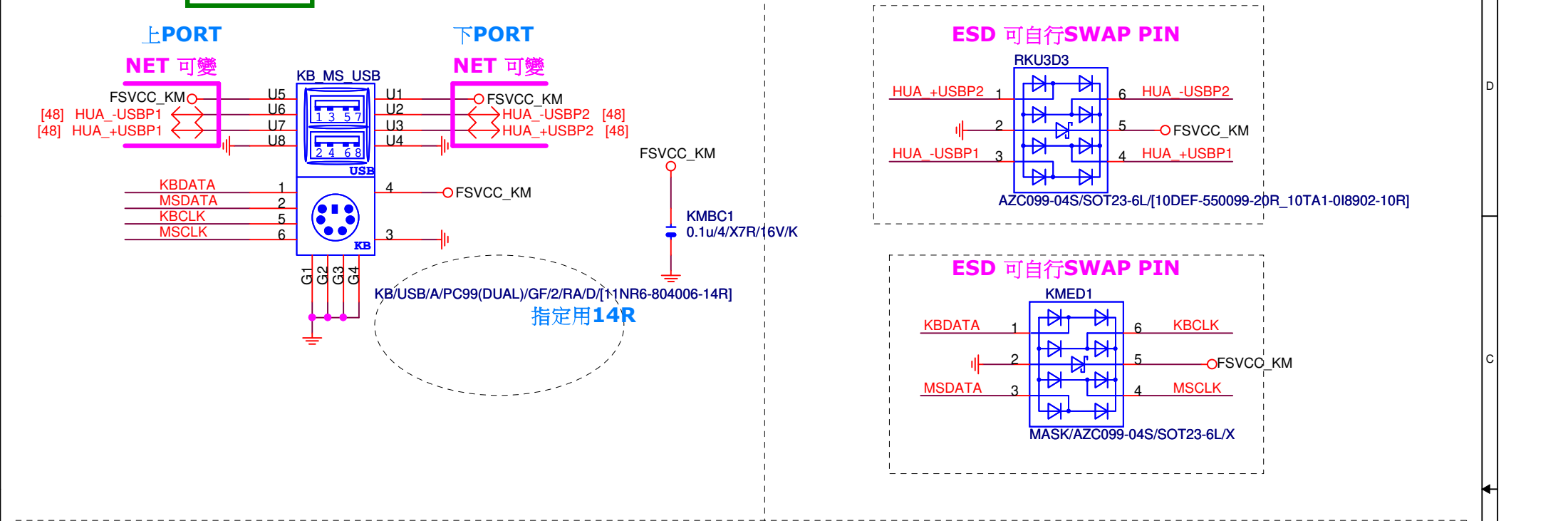


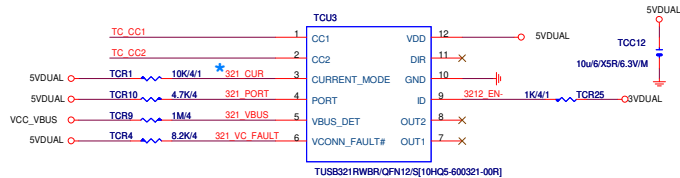
Close to connector
FUSE 2 Port 1 Fuse 2A



Gigabyte Technology

Title			
USB2.0			
Size	Document Number	Rev	
Custom	Z590 UD AC	1.0	
Date:	Friday, December 11, 2020	Sheet	50 of 69





CURRENT MODE

L - Default current / Pull down to GND or NC
M - Medium (1.5A) current / Pull up to VDD 500K
H - High (3.0A) current / Pull up to VDD 10K

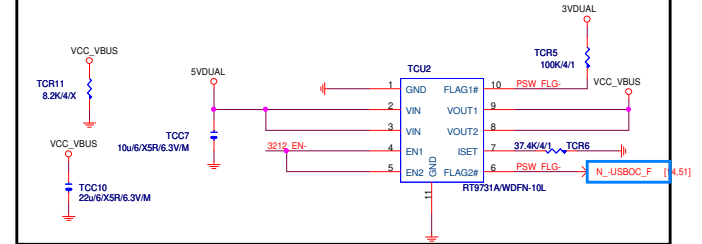
PORT

H - HOST
L - Device
NC - Dual Role

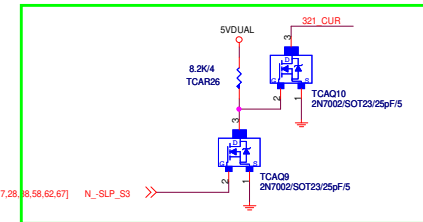
USB POWER

note: 可變更FUSB

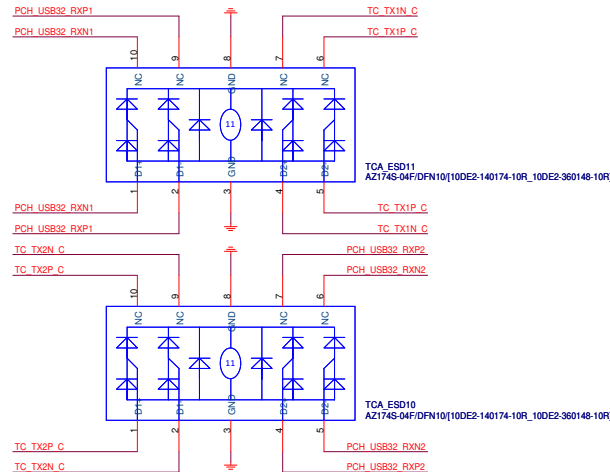
TypeC default 5V/3A



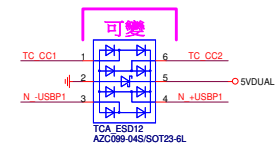
For VBUS current limit at 900mA on S3



Color markers can be changed by model



note: 可變更USB NAME

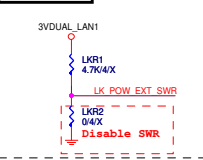


USB2.0 can be used the same source

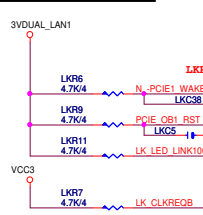
Gigabyte Technology

Title		
R_USB30,USB_OC		
Size	Document Number	Rev
C	Z590 UD AC	1.0
Date:	Friday, December 11, 2020	Sheet S3 of 69

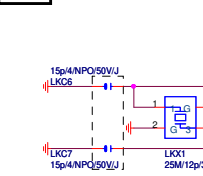
POW_MODE



External Resistor



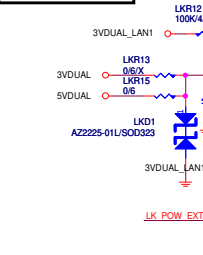
25M SMD Type



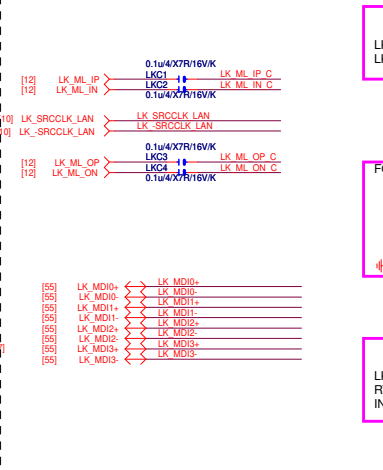
SWR



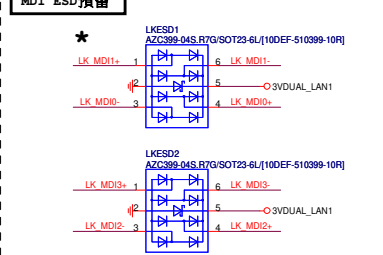
EXTERNAL (0.9V)



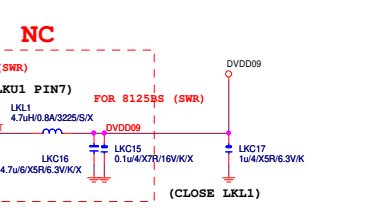
External SWR for RTL8125BS SWR disabled



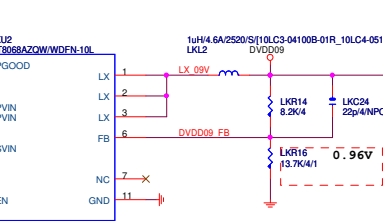
MDI ESD 預留



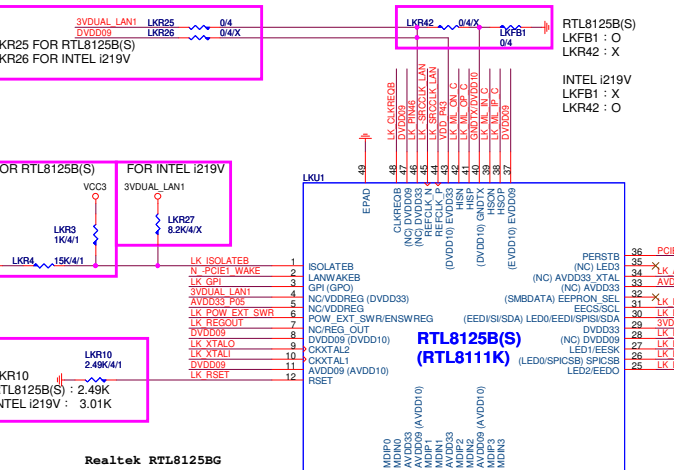
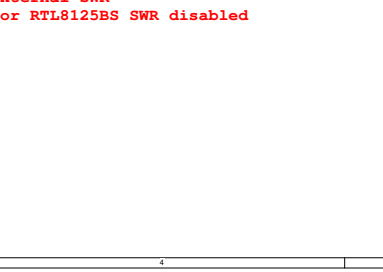
LAN POWER



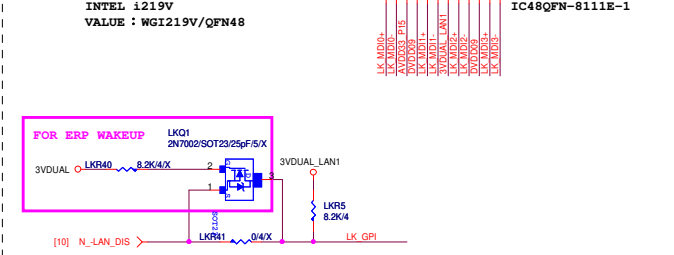
LAN POWER



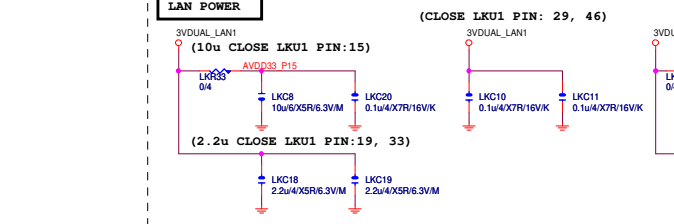
LAN POWER



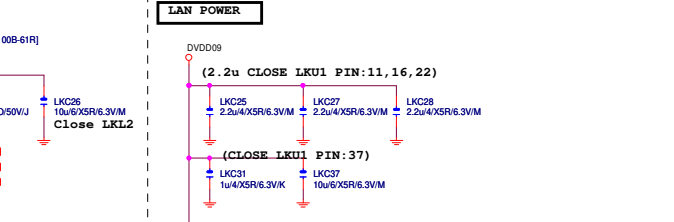
LAN POWER



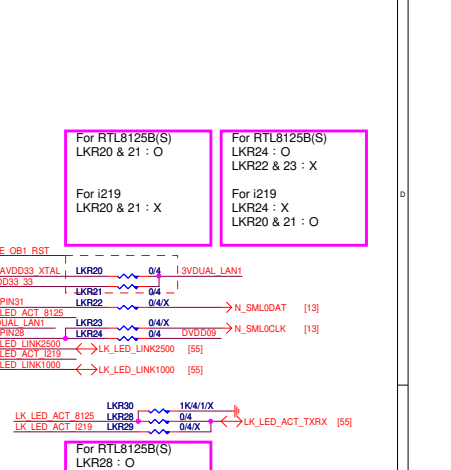
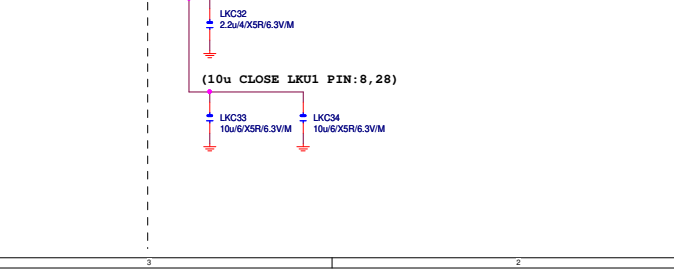
LAN POWER



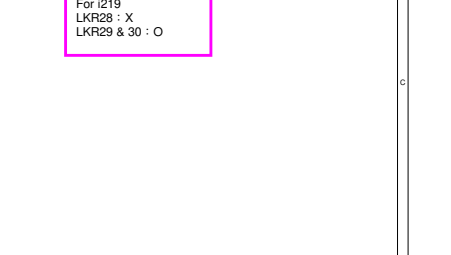
LAN POWER



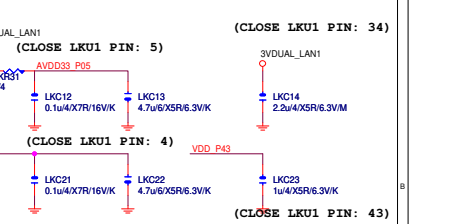
LAN POWER



LAN POWER



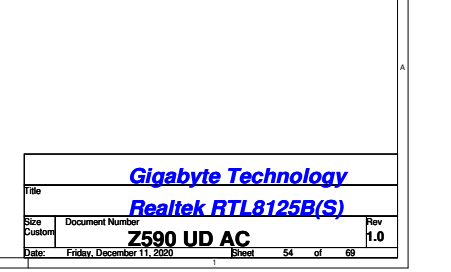
LAN POWER



LAN POWER

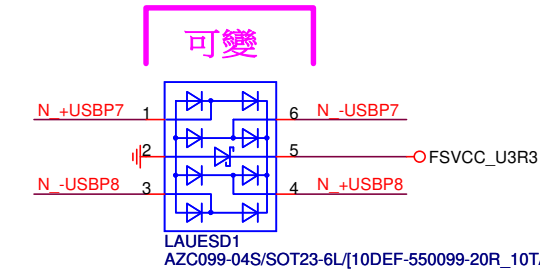


LAN POWER

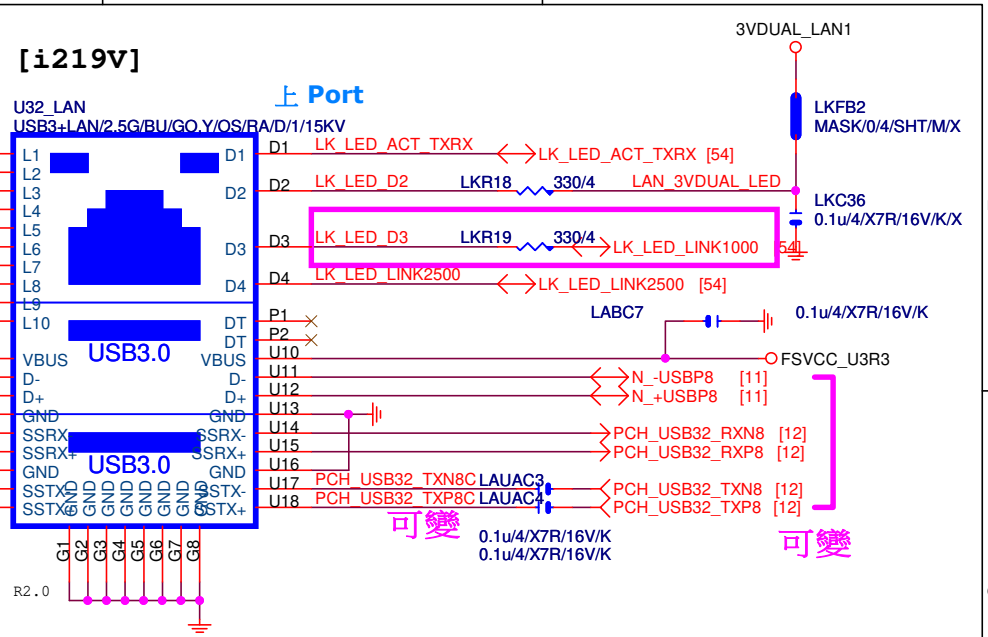
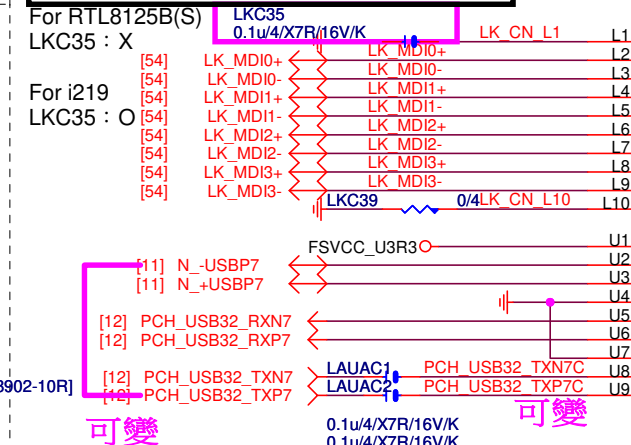


USB_LAN CONNECTOR R0.3

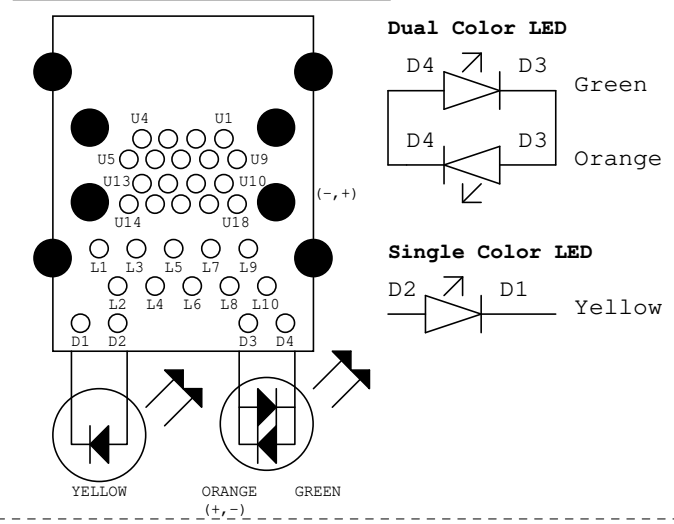
RMA ESD PROTECT note:可變更USB NAME



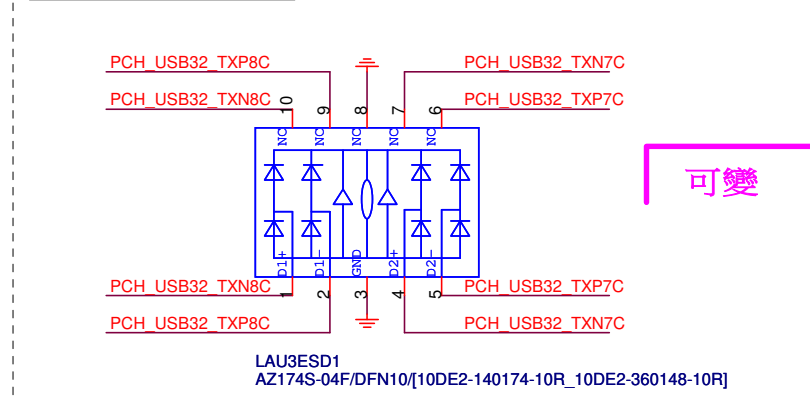
USB_LAN CONNECTOR LA_MDI-->100歐姆: [20/4/8/4/20]



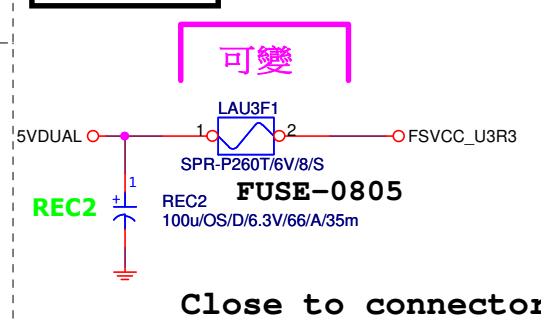
USB30_LAN LAYOUT示意圖



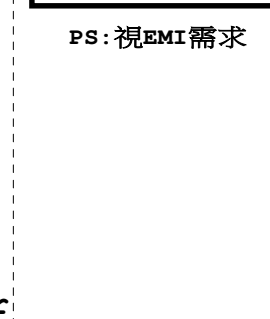
RMA ESD PROTECT note:可變更USB NAME



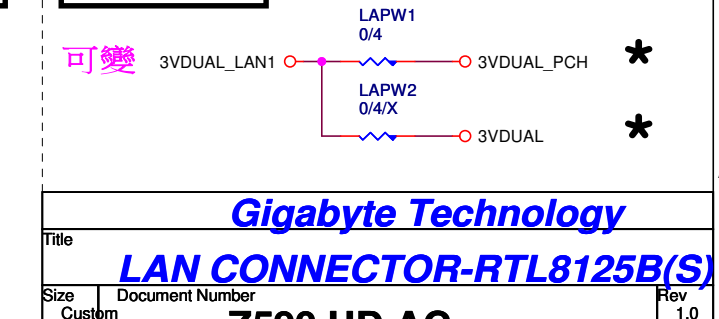
USB POWER note:可變更FUSE



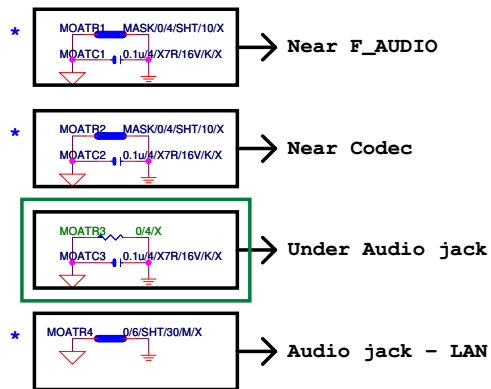
EMI SHORT PAD PS:視EMI需求



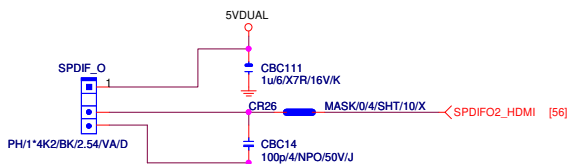
LAN POWER note: lan power連接及電流



Rev 6.0

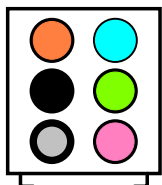


*量産前,MOATR1/MOATR2/MOATR40ohm改short pad



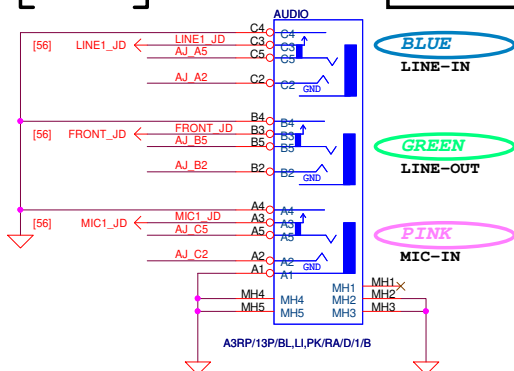
For HDMI SPDIF (依SPEC保留或移除)

AZALIA JACK

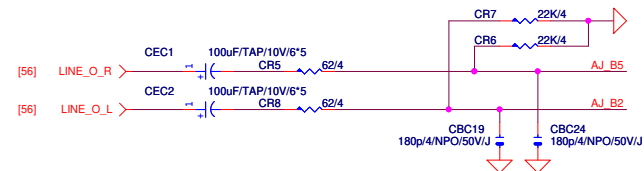


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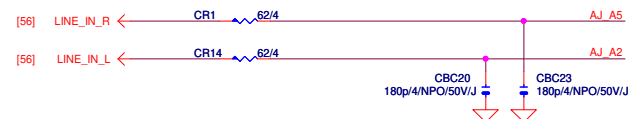
AZALIA JACK



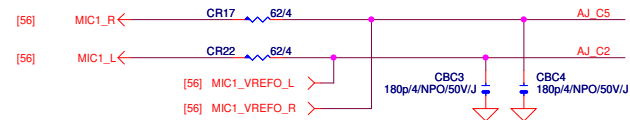
LINE-OUT



LINE-IN



MIC-IN

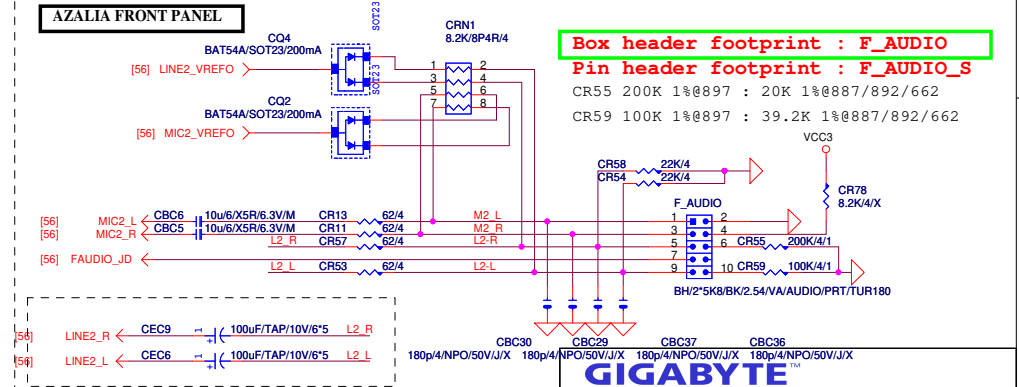


SURROUND

CEN/LFE

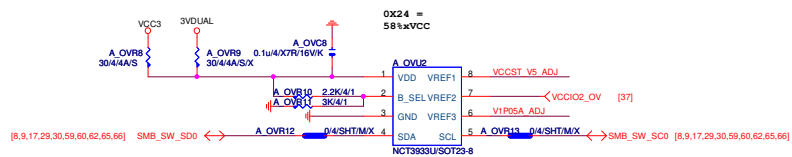
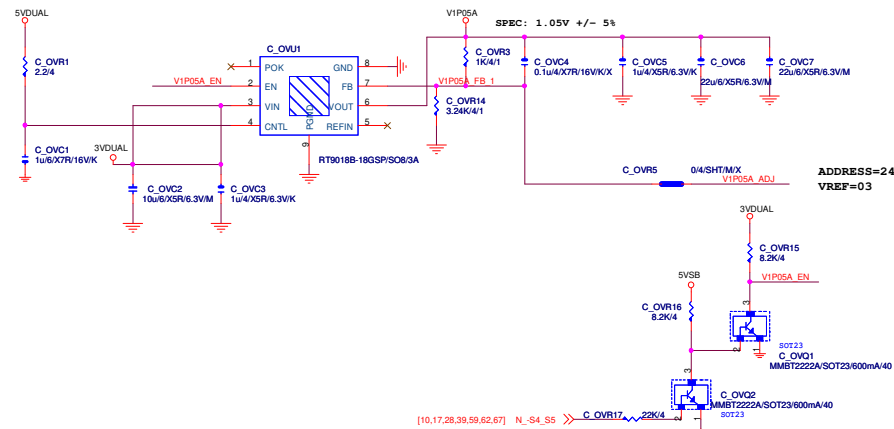
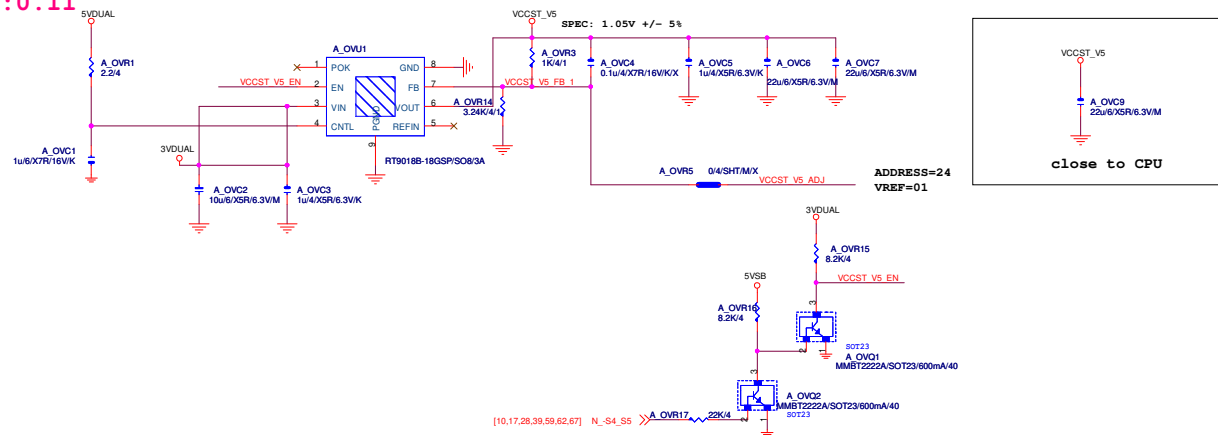
SURR BACK

AZALIA FRONT PANEL

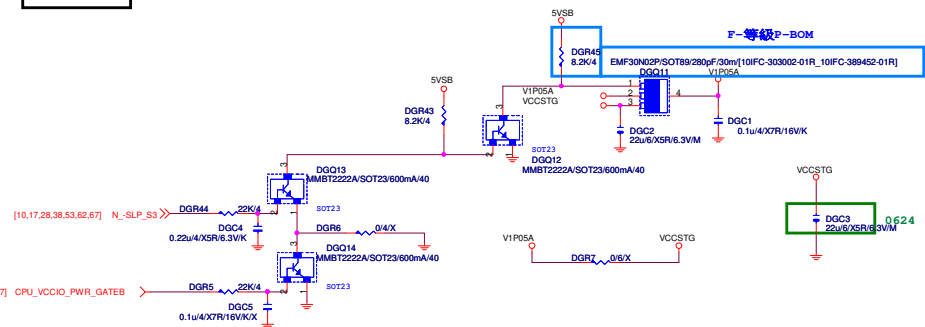


GIGABYTE

Title		
AUDIO JACK		
Size	Document Number	Rev
Custom	Z590 UD AC	1.0
Date:	Friday, December 11, 2020	Sheet 57 of 69



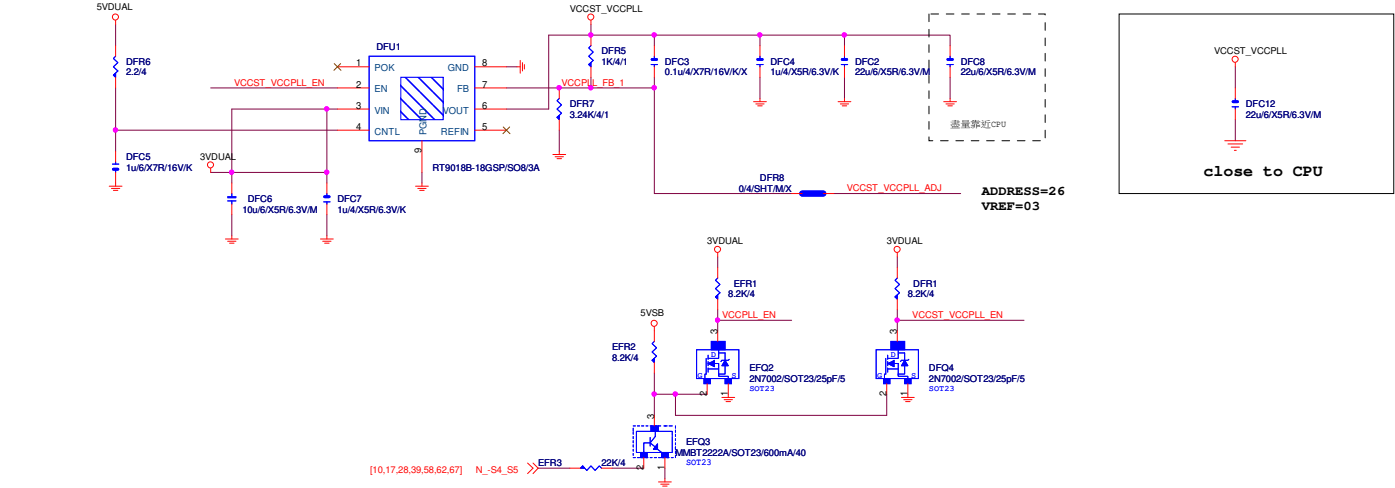
VCCSTG



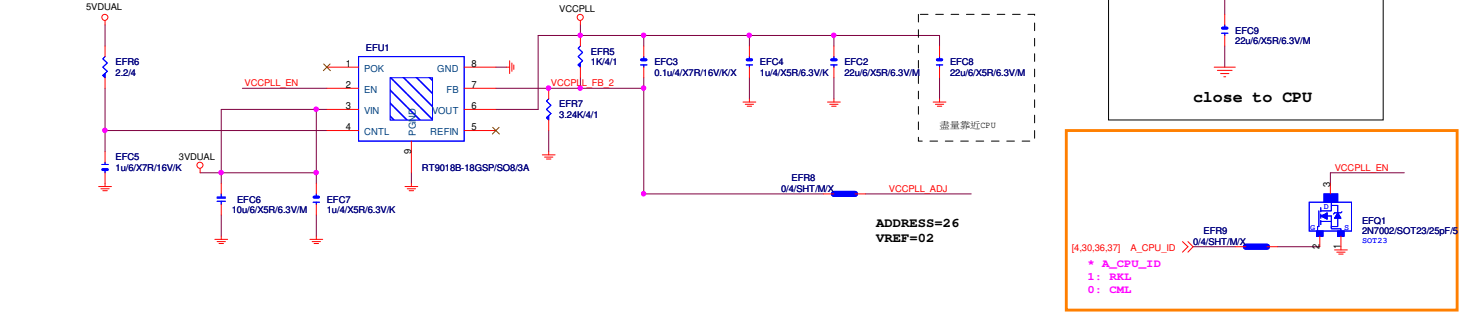
GIGABYTE™

Title			
CPU POWER-1			
Size	Document Number		Rev
Custom	Z590 UD AC		1.0
Date:	Friday, December 11, 2020	Sheet	58 of 69

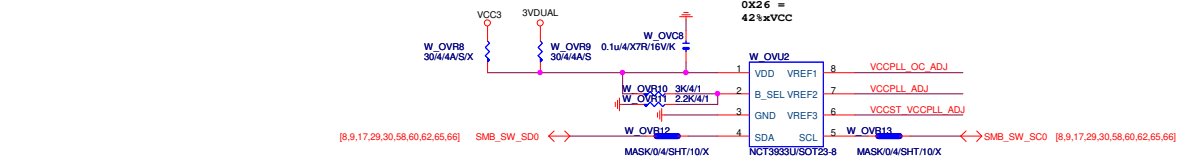
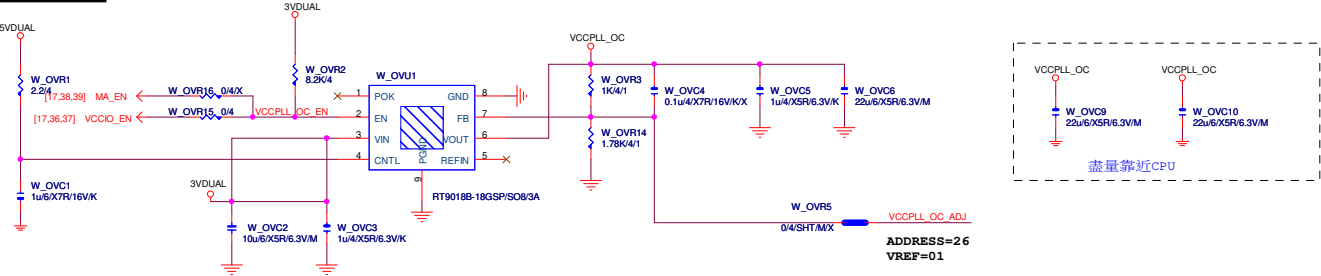
VCCST_VCCPLL 替換原先MOS開關線路



VCCPLL

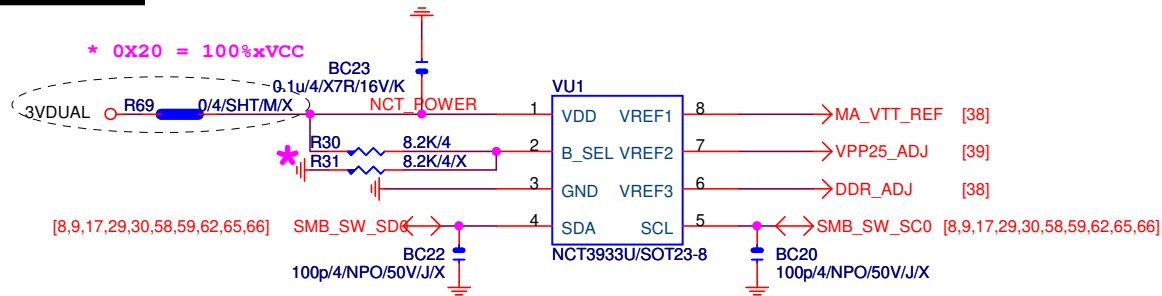


VCCPLL_OC



OVER VOLTAGE

REV: 0.11



NCT3933	0X2A	0X20
VREF1	VCC18_PCH	DDRVTT
VREF2	VCCIO	VPP25V
VREF3	VCC1V8_PRIM	VDDQ

Gigabyte Technology

Title

CPU CORE VR-2

Size
Custom

Document Number

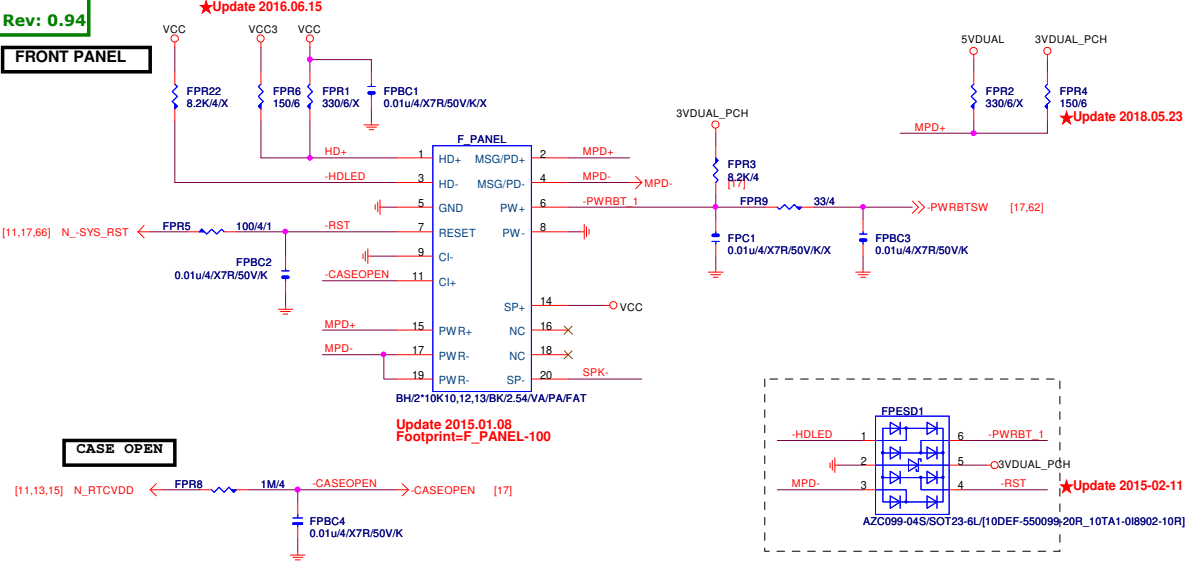
Z590 UD AC

Rev
1.0

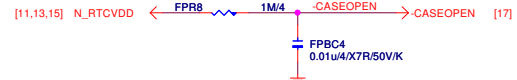
Date: Friday, December 11, 2020

Sheet	60	of	69
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FRONT PANEL

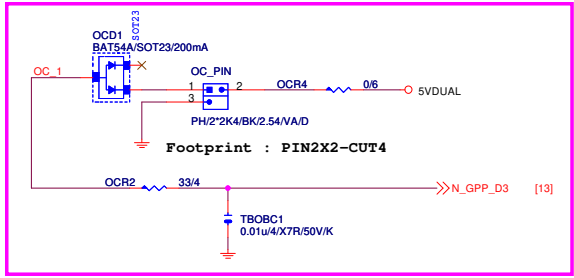


CASE OPEN

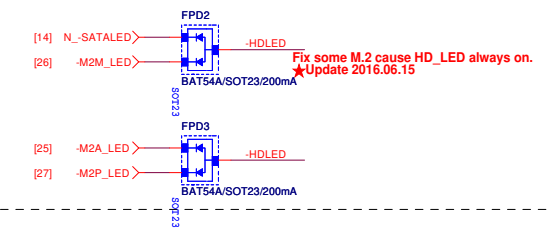


FRONT PANEL SHORT

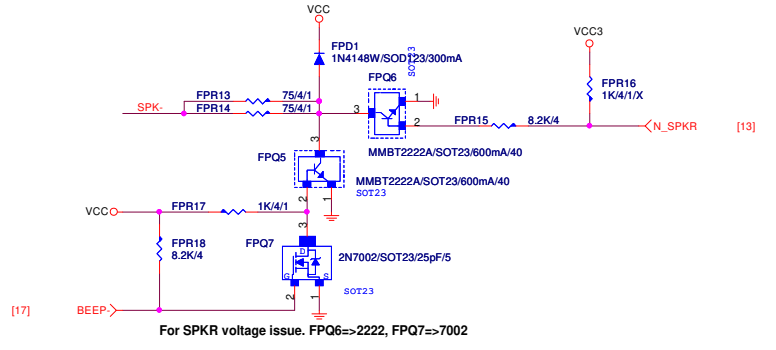
* FOR 客户Button



SATA/M.2 LED

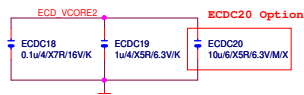
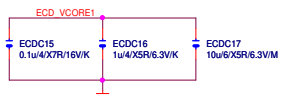
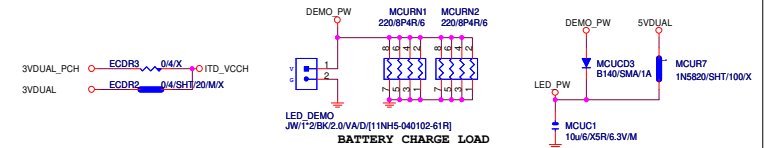
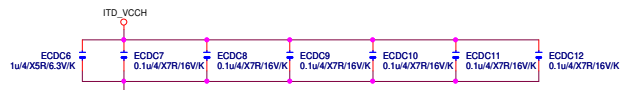
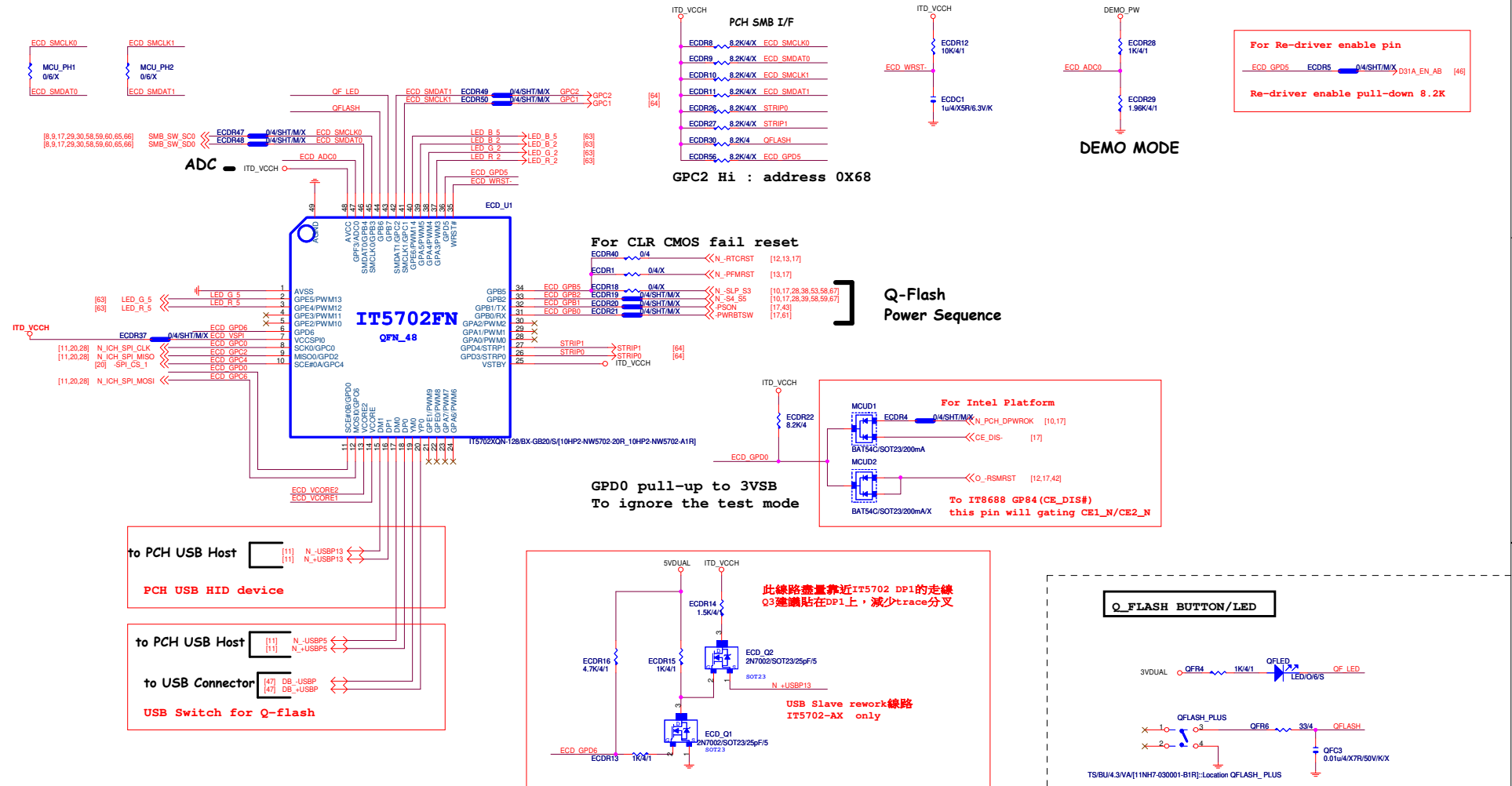


SPKR W/O EC



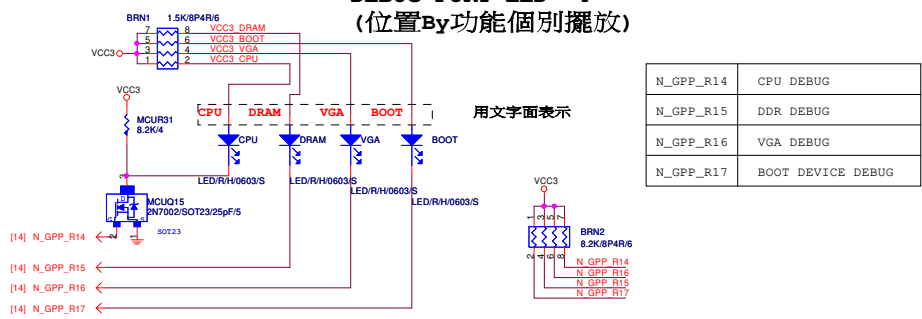
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ECD_U1 請放在PCH到BIOS路徑上.避免線過長



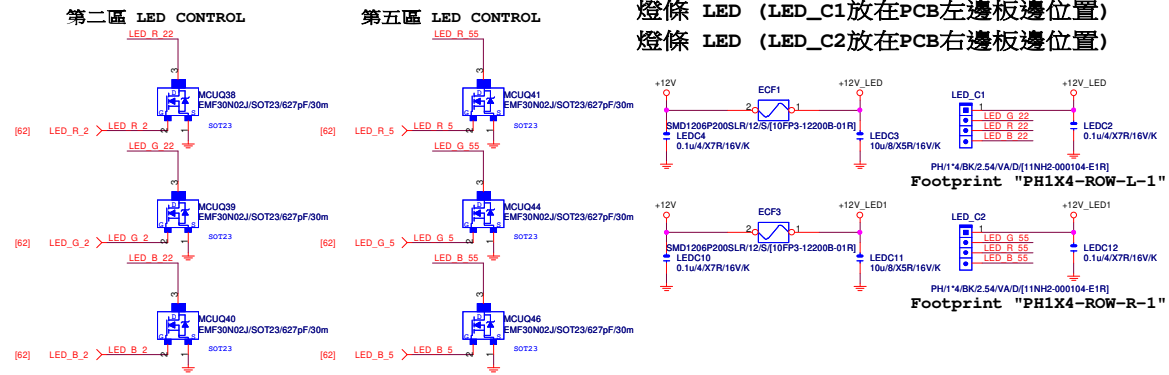
第一區 LED

DEBUG PORT LED *4
(位置By功能個別擺放)



第三區 LED

第五區 LED



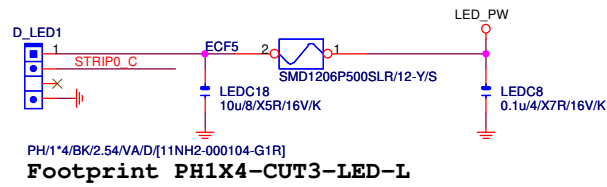
第四區 LED

GIGABYTE™

File			PCH/AUDIO/DEBUG/C_LED1/2
Size	Document Number	Rev	1.0
Custom	Z590 UD AC		
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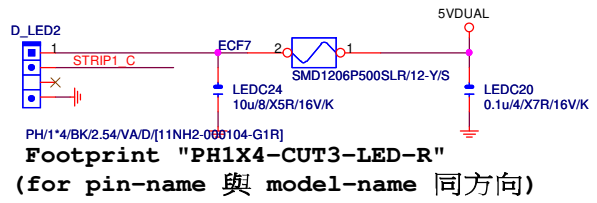
第六區 LED (靠近左上板邊位置)

Digital LED Strip1

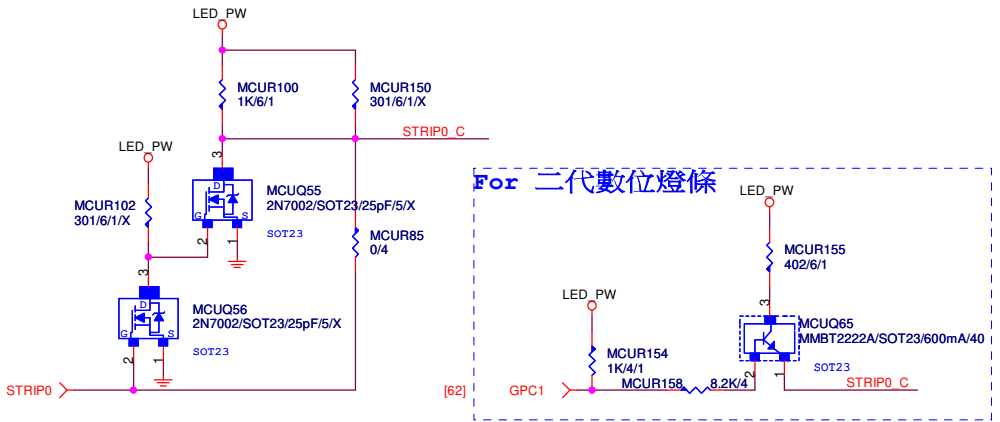


第七區 (靠近右下CPU板邊位置)

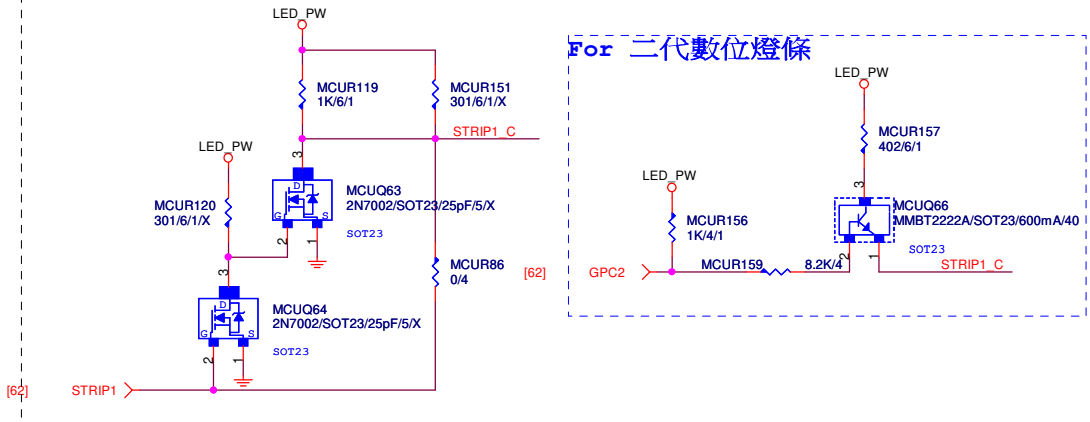
Digital LED Strip2



燈條 Level shift



燈條 Level shift



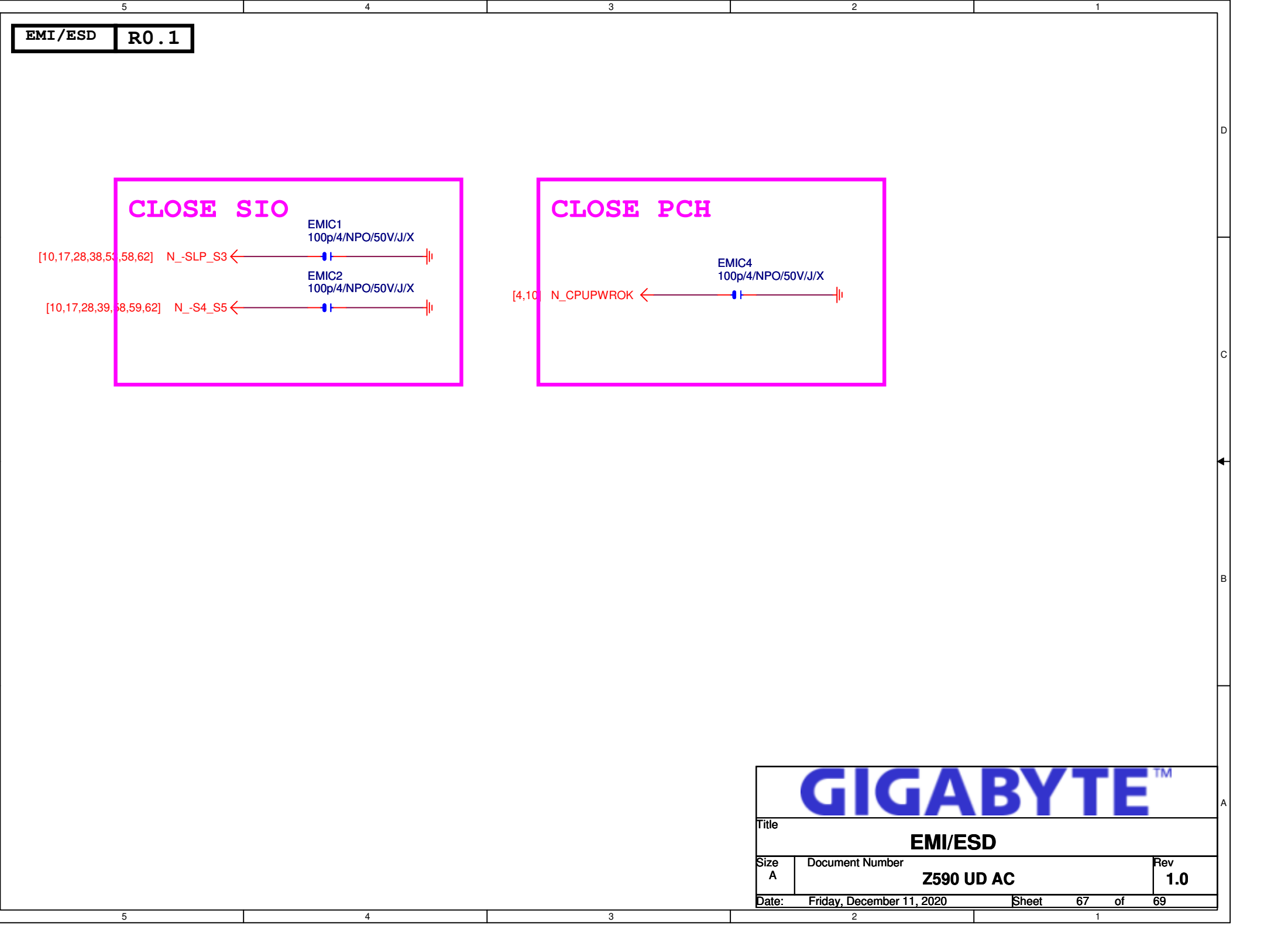
***量産時，全部不上件**

INTERNAL

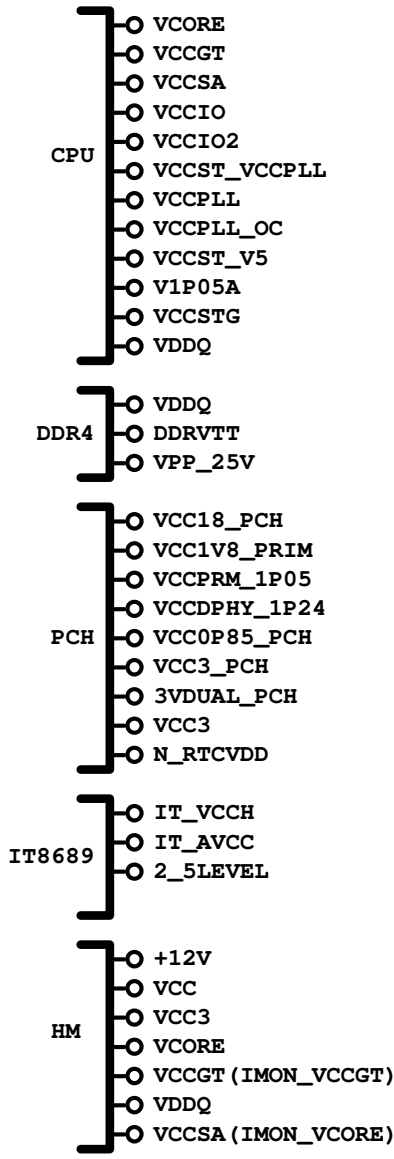


GIGABYTE™

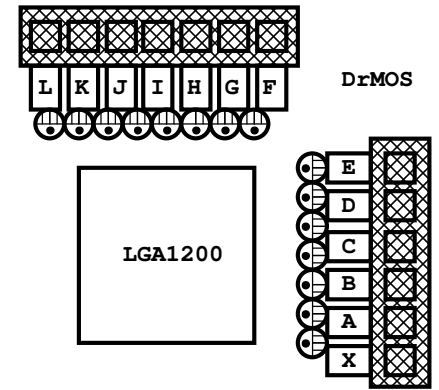
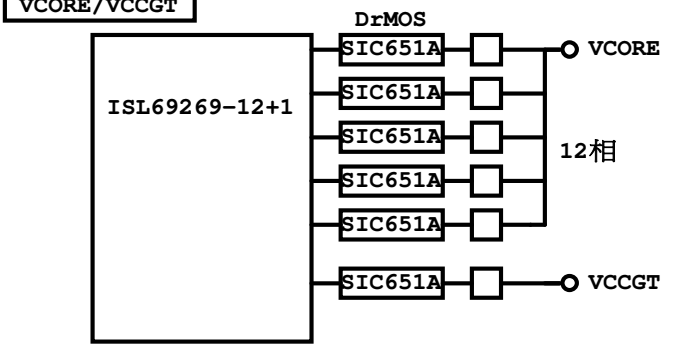
Title			
IDT6V41801			
Size	Document Number	Rev	
Custom	Z590 UD AC	1.0	
Date:	Friday, December 11, 2020	Sheet	66 of 69



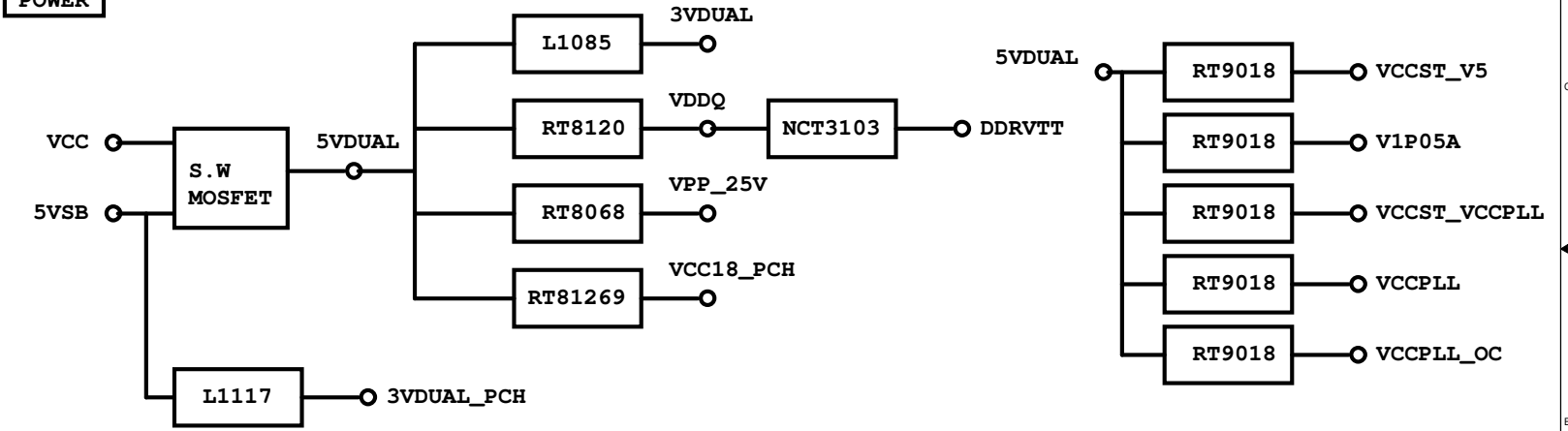
POWER BLOCK MAP



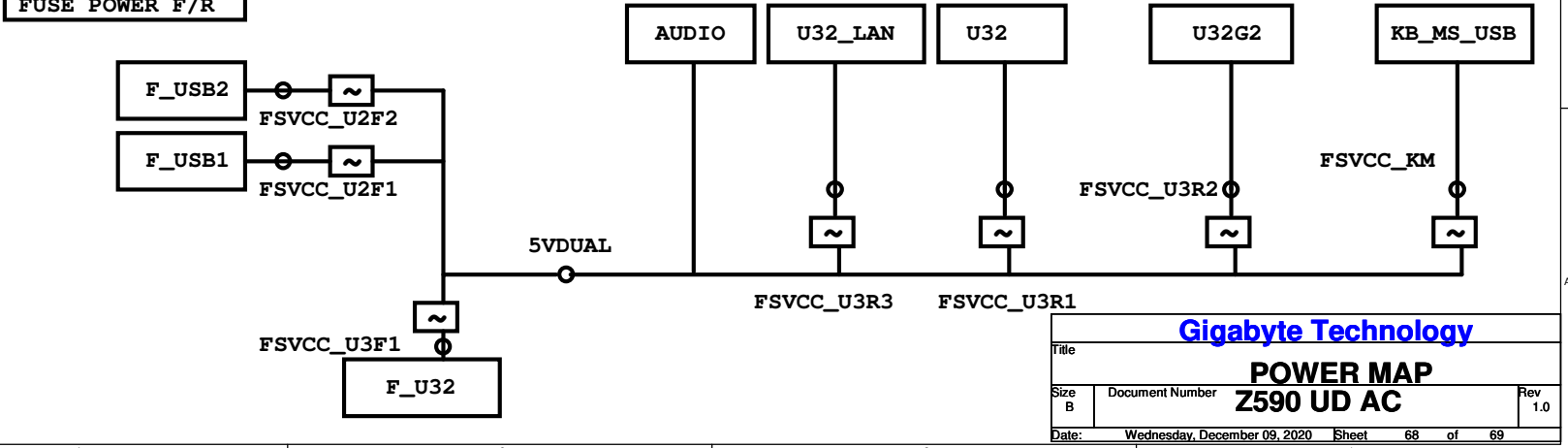
VCORE/VCCGT

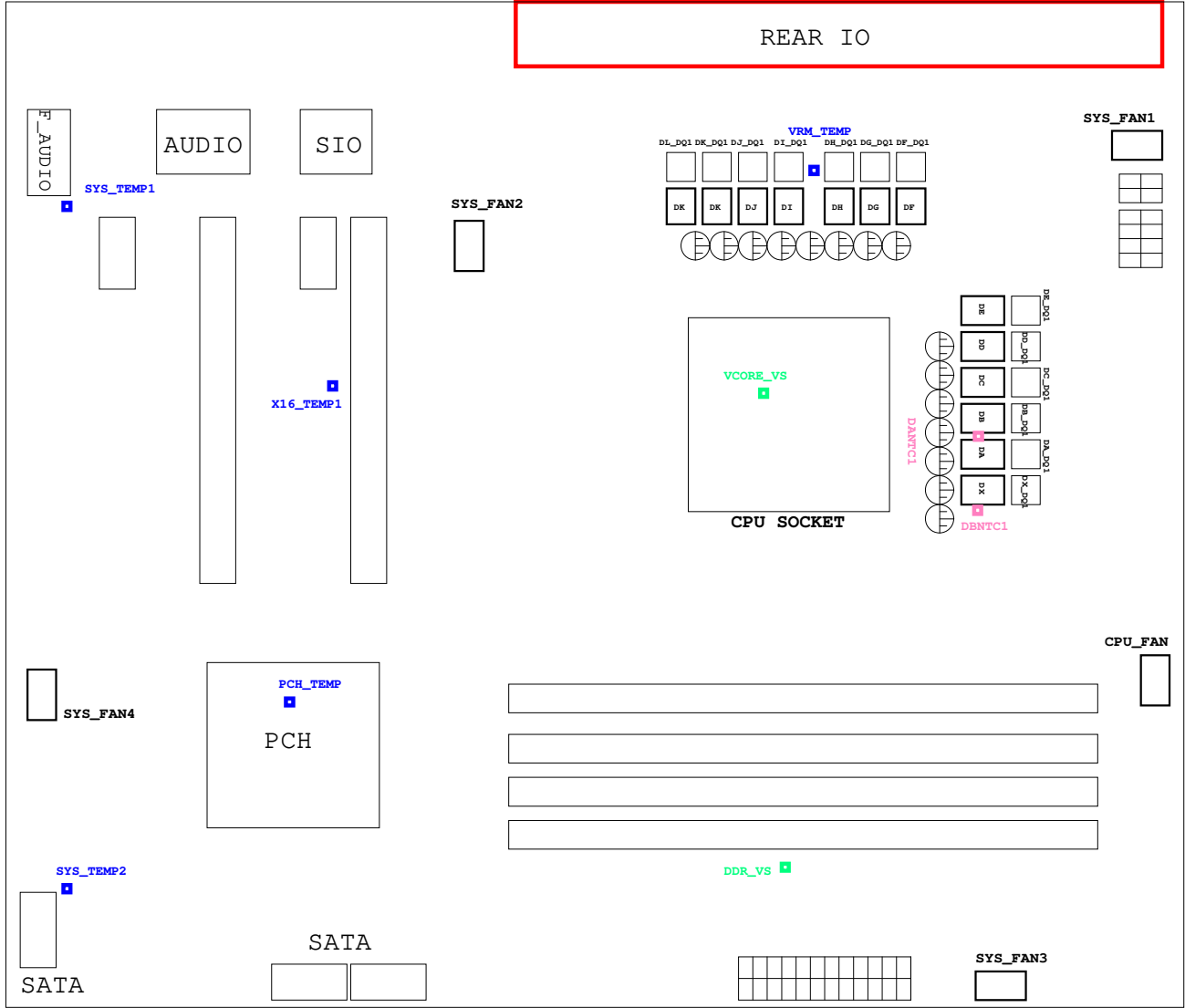


POWER



FUSE POWER F/R





熱敏電阻	擺放靠近位置	走線方式
DANTC1	DB_DL1	Differential
DBNTC1	DX_DL1	Differential
VRM_TEMP	DC_DQ1	N/A
X16_TEMP1	PCIEX16	N/A
PCH_TEMP	PCH	N/A
SYS_TEMP1	F_AUDIO	N/A
SYS_TEMP2	F_PANEL	N/A

- SIO RS
- PWM RS
- SIO VIN



FAN